

## TL07xx Low-Noise JFET-Input Operational Amplifiers

### 1 Features

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion: 0.003% (Typical)
- Low Noise  
 $V_n = 18 \text{ nV}/\sqrt{\text{Hz}}$  (Typical) at  $f = 1 \text{ kHz}$
- High-Input Impedance: JFET Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate:  $13 \text{ V}/\mu\text{s}$  (Typical)
- Common-Mode Input Voltage Range Includes  $V_{CC+}$

### 2 Applications

- Motor Integrated Systems: UPS
- Drives and Control Solutions: AC Inverter and VF Drives
- Renewables: Solar Inverters
- Pro Audio Mixers
- DLP Front Projection System
- Oscilloscopes

### 3 Description

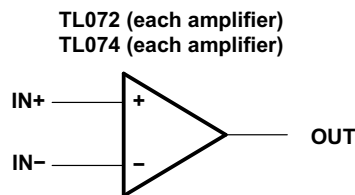
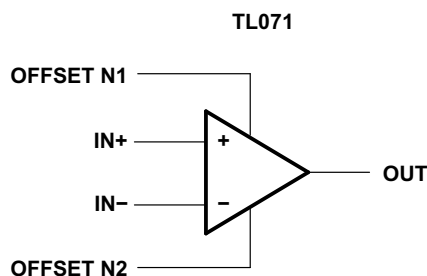
The TL07xx JFET-input operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low-input bias and offset currents, and low offset-voltage temperature coefficient. The low harmonic distortion and low noise make the TL07x series ideally suited for high-fidelity and audio pre-amplifier applications. The TL071 device has offset pins to support external input offset correction.

Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL07xxD	SOIC (14)	8.65 mm x 3.91 mm
	SOIC (8)	4.90 mm x 3.90 mm
TL07xxJG	CDIP (8)	9.59 mm x 6.67 mm
TL074xJ	CDIP (14)	19.56 mm x 6.92 mm
TL07xxP	PDIP (8)	9.59 mm x 6.35 mm
TL07xxPS	SO (8)	6.20 mm x 5.30 mm
TL074xN	PDIP (14)	19.3 mm x 6.35 mm
TL074xNS	SO (14)	10.30 mm x 5.30 mm
TL07xxPW	TSSOP (8)	4.40 mm x 3.00 mm
TL074xPW	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Logic Symbols



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (February 2014) to Revision N	Page
• Updated data sheet text to latest documentation and translation standards .....	<b>1</b>
• Added TL072M and TL074M devices to data sheet .....	<b>1</b>
• Rewrote text in <i>Description</i> section .....	<b>1</b>
• Changed TL07x 8-pin PDIP package to 8-pin CDIP package in <i>Device Information</i> table .....	<b>1</b>
• Deleted 20-pin LCCC package from <i>Device Information</i> table .....	<b>1</b>
• Added 2017 copyright statement to front page schematic .....	<b>1</b>
• Deleted TL071x FK (LCCC) pinout drawing and pinout table in <i>Pin Configurations and Functions</i> section .....	<b>4</b>
• Updated pinout diagrams and pinout tables in <i>Pin Configurations and Functions</i> section .....	<b>5</b>
• Deleted differential input voltage parameter from <i>Absolute Maximum Ratings</i> table .....	<b>10</b>
• Deleted table notes from <i>Absolute Maximum Ratings</i> table .....	<b>10</b>
• Added new table note to <i>Absolute Maximum Ratings</i> table .....	<b>10</b>
• Changed minimum supply voltage value from –18 V to –0.3 V in <i>Absolute Maximum Ratings</i> table .....	<b>10</b>
• Changed maximum supply voltage from 18 V to 36 V in <i>Absolute Maximum Ratings</i> table .....	<b>10</b>
• Changed minimum input voltage value from –15 V to $V_{CC-} - 0.3$ V in <i>Absolute Maximum Ratings</i> table .....	<b>10</b>
• Changed maximum input voltage from 15 V to $V_{CC+} + 36$ V in <i>Absolute Maximum Ratings</i> table .....	<b>10</b>
• Added input clamp current parameter to <i>Absolute Maximum Ratings</i> table .....	<b>10</b>
• Changed common-mode voltage maximum value from $V_{CC+} - 4$ V to $V_{CC+}$ in the <i>Recommended Operating Conditions</i> table .....	<b>10</b>

**Revision History (continued)**

• Changed devices in <i>Recommended Operating Conditions</i> table from TL07xA and TL07xB to TL07xAC and TL07xBC .....	10
• Added TL07xI operating free-air temperature minimum value of –40°C to <i>Recommended Operating Conditions</i> table ...	10
• Added U (CFP) package thermal values to <i>Thermal Information: TL072x (cont.)</i> table .....	11
• Added W (CFP) package thermal values to <i>Thermal Information: TL074x (cont.)</i> table .....	12
• Added <a href="#">Figure 20</a> to <a href="#">Table 1</a> .....	20
• Added <a href="#">Figure 20</a> to <i>Typical Characteristics</i> section .....	24
• Added second <i>Typical Application</i> section application curves .....	29
• Reformatted document references in <i>Layout Guidelines</i> section .....	32
• Updated formatting of document reference in <i>Related Documentation</i> section .....	34

**Changes from Revision L (February 2014) to Revision M**
**Page**

• Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes, Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section .....	1
• Moved <i>Typical Characteristics</i> into <i>Specifications</i> section. ....	20

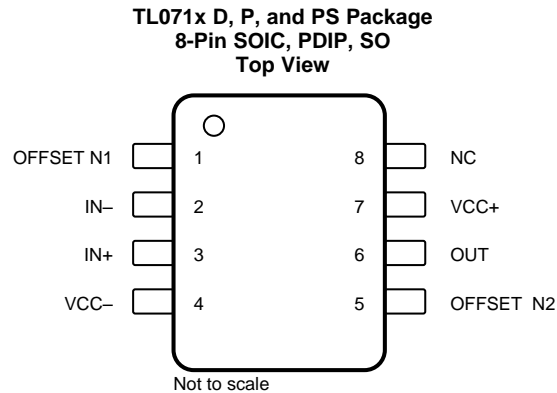
**Changes from Revision K (January 2014) to Revision L**
**Page**

• Moved $T_{stg}$ to <i>Handling Ratings</i> table .....	10
• Added <i>Device and Documentation Support</i> section .....	34
• Added <i>Mechanical, Packaging, and Orderable Information</i> section .....	34

**Changes from Revision J (March 2005) to Revision K**
**Page**

• Updated document to new TI datasheet format - no specification changes. ....	1
• Added ESD warning .....	34

## 5 Pin Configuration and Functions

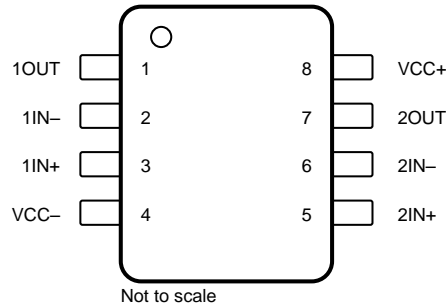


NC- no internal connection

**Pin Functions: TL071x**

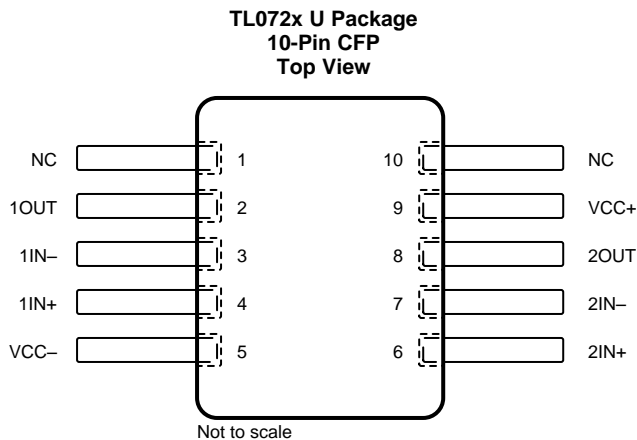
PIN		I/O	DESCRIPTION
NAME	NO.		
IN-	2	I	Inverting input
IN+	3	I	Noninverting input
NC	8	—	Do not connect
OFFSET N1	1	—	Input offset adjustment
OFFSET N2	5	—	Input offset adjustment
OUT	6	O	Output
VCC-	4	—	Power supply
VCC+	7	—	Power supply

**TL072x D, JG, P, PS and PW Package  
8-Pin SOIC, CDIP, PDIP, SO  
Top View**



**Pin Functions: TL072x**

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN-	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN-	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
VCC-	4	—	Power supply
VCC+	8	—	Power supply

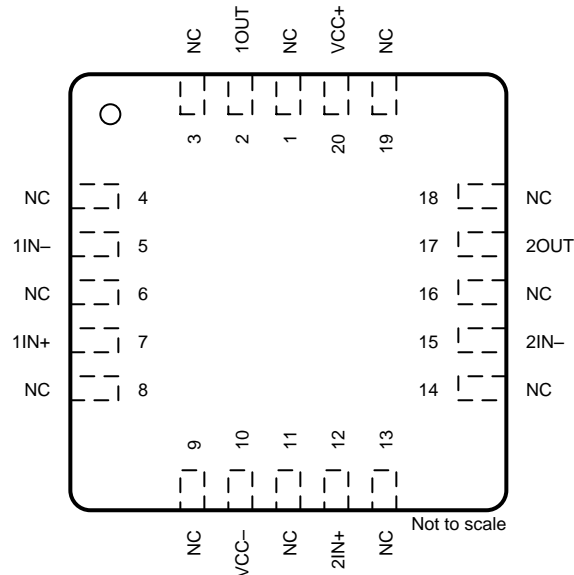


NC- no internal connection

**Pin Functions: TL072x**

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN-	3	I	Inverting input
1IN+	4	I	Noninverting input
1OUT	2	O	Output
2IN-	7	I	Inverting input
2IN+	6	I	Noninverting input
2OUT	8	O	Output
NC	1, 10	—	Do not connect
VCC-	5	—	Power supply
VCC+	9	—	Power supply

**TL072 FK Package  
20-Pin LCCC  
Top View**

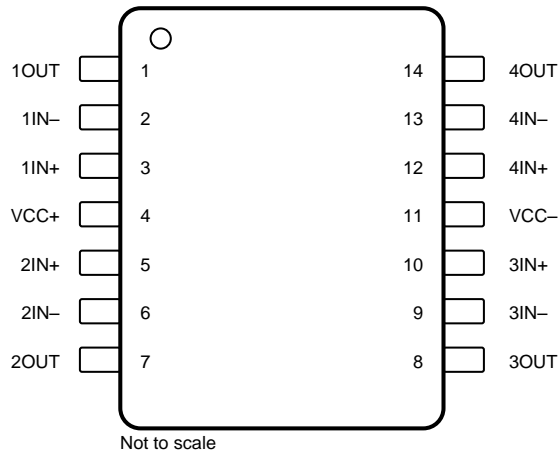


NC- no internal connection

**Pin Functions: TL072x**

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN-	5	I	Inverting input
1IN+	7	I	Noninverting input
1OUT	2	O	Output
2IN-	15	I	Inverting input
2IN+	12	I	Noninverting input
2OUT	17	O	Output
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	Do not connect
VCC-	10	—	Power supply
VCC+	20	—	Power supply

TL074 D, N, NS, PW, J, and W Packages  
 14-Pin SOIC, PDIP, SO, TSSOP, CDIP and CFP  
 Top View

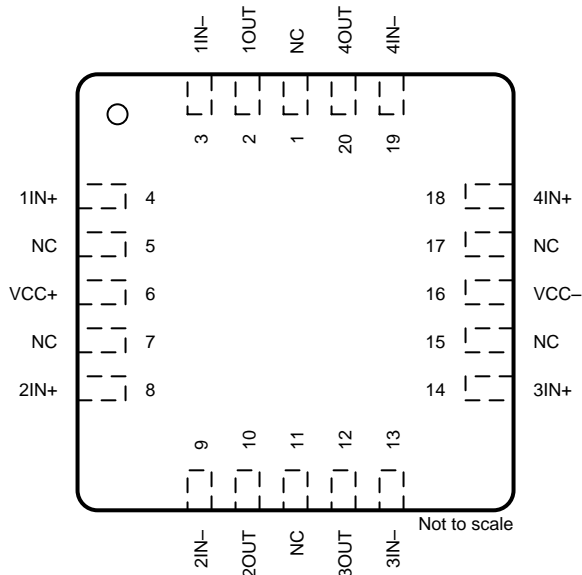


Pin Functions: TL074x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN-	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN-	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
3IN-	9	I	Inverting input
3IN+	10	I	Noninverting input
3OUT	8	O	Output
4IN-	13	I	Inverting input
4IN+	12	I	Noninverting input
4OUT	14	O	Output
V <sub>CC-</sub>	11	—	Power supply
V <sub>CC+</sub>	4	—	Power supply



**TL074 FK Package  
20-Pin LCCC  
Top View**



NC- no internal connection

**Pin Functions: TL074x**

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN-	3	I	Inverting input
1IN+	4	I	Noninverting input
1OUT	2	O	Output
2IN-	9	I	Inverting input
2IN+	8	I	Noninverting input
2OUT	10	O	Output
3IN-	13	I	Inverting input
3IN+	14	I	Noninverting input
3OUT	12	O	Output
4IN-	19	I	Inverting input
4IN+	18	I	Noninverting input
4OUT	20	O	Output
NC	1, 5, 7, 11, 15, 17	—	Do not connect
VCC-	16	—	Power supply
VCC+	6	—	Power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage	-0.3	36	V
$V_I$	Input voltage <sup>(2)</sup>	$V_{CC-} - 0.3$	$V_{CC-} + 36$	V
$I_{IK}$	Input clamp current		-50	mA
	Duration of output short circuit <sup>(3)</sup>	Unlimited		
$T_J$	Operating virtual junction temperature		150	°C
	Case temperature for 60 seconds - FK package		260	°C
	Lead temperature 1.8 mm (1/16 inch) from case for 10 seconds		300	°C
$T_{stg}$	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Differential voltage only limited by input voltage.
- (3) The output may be shorted to ground or to either supply. Temperature and supply voltages must be limited to ensure that the dissipation rating is not exceeded.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
$V_{CC+}$	Supply voltage <sup>(1)</sup>	5	15	V	
$V_{CC-}$	Supply voltage <sup>(1)</sup>	-5	-15	V	
$V_{CM}$	Common-mode voltage	$V_{CC-} + 4$	$V_{CC+}$	V	
$T_A$	Operating free-air temperature	TL07xM	-55	125	°C
		TL08xQ	-40	125	
		TL07xI	-40	85	
		TL07xAC, TL07xBC, TL07xC	0	70	

- (1)  $V_{CC+}$  and  $V_{CC-}$  are not required to be of equal magnitude, provided that the total  $V_{CC}$  ( $V_{CC+} - V_{CC-}$ ) is between 10 V and 30 V.

#### 6.4 Thermal Information: TL071x

THERMAL METRIC <sup>(1)</sup>		TL071x			UNIT
		D (SOIC)	P (PDIP)	PS (SO)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	85	95	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

#### 6.5 Thermal Information: TL072x

THERMAL METRIC <sup>(1)</sup>		TL072x				UNIT
		D (SOIC)	JG (CDIP)	P (PDIP)	PS (SO)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	—	85	95	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	15.05	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

#### 6.6 Thermal Information: TL072x (cont.)

THERMAL METRIC <sup>(1)</sup>		TL072x			UNIT
		PW (TSSOP)	U (CFP)	FK (LCCC)	
		8 PINS	10 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	169.8	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	62.1	5.61	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	176.2	—	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	—	48.4	—	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	—	144.1	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	5.4	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

#### 6.7 Thermal Information: TL074x

THERMAL METRIC <sup>(1)</sup>		TL074x			UNIT
		D (SOIC)	N (PDIP)	NS (SO)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	80	76	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 6.8 Thermal Information: TL074x (cont).

THERMAL METRIC <sup>(1)</sup>	TL074x			UNIT
	J (CDIP)	PW (TSSOP)	W (CFP)	
	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	—	113	128.8	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	14.5	—	56.1	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	—	—	127.6	°C/W
$\psi_{JT}$ Junction-to-top characterization parameter	—	—	29	°C/W
$\psi_{JB}$ Junction-to-board characterization parameter	—	—	106.1	°C/W
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	—	—	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 6.9 Thermal Information: TL074x (cont).

THERMAL METRIC <sup>(1)</sup>	TL074x		UNIT
	FK (LCCC)		
	20 PINS		
$R_{\theta JA}$ Junction-to-ambient thermal resistance	—		°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	5.61		°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.10 Electrical Characteristics: TL071C, TL072C, TL074C

 $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup> <sup>(2)</sup>		MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		3	10	mV
			$T_A = \text{Full range}$			13	
$\alpha$	Temperature coefficient of input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = \text{Full range}$		18		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$	Input offset current	$V_O = 0$	$T_A = 25^\circ\text{C}$		5	100	pA
			$T_A = \text{Full range}$				10
$I_{IB}$	Input bias current <sup>(3)</sup>	$V_O = 0$	$T_A = 25^\circ\text{C}$		65	200	pA
			$T_A = \text{Full range}$				7
$V_{ICR}$	Common-mode input voltage range	$T_A = 25^\circ\text{C}$		$\pm 11$	–12 to 15		V
$V_{OM}$	Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$	$\pm 12$	$\pm 13.5$		V
		$R_L \geq 10\ \text{k}\Omega$	$T_A = \text{Full range}$	$\pm 12$			
		$R_L \geq 2\ \text{k}\Omega$		$\pm 10$			
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}$ $R_L \geq 2\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$	25	200		V/mV
			$T_A = \text{Full range}$	15			
$B_1$	Utility-gain bandwidth	$T_A = 25^\circ\text{C}$			3		MHz
$r_i$	Input resistance	$T_A = 25^\circ\text{C}$			$10^{12}$		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(\text{min})}$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	70	100		dB
$k_{SVR}$	Supply voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = \pm 9\ \text{V}$ to $\pm 15\ \text{V}$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	70	100		dB
$I_{CC}$	Supply current (each amplifier)	$V_O = 0$ ; no load			1.4	2.5	mA
$V_{O1} / V_{O2}$	Crosstalk attenuation	$A_{VD} = 100$			120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.

(2) Full range is  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ .

(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 1](#). Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

## 6.11 Electrical Characteristics: TL071AC, TL072AC, TL074AC

$V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup> <sup>(2)</sup>		MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		3	6	mV
			$T_A = \text{Full range}$			7.5	
$\alpha$	Temperature coefficient of input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = \text{Full range}$		18		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$	Input offset current	$V_O = 0$	$T_A = 25^\circ\text{C}$		5	100	pA
			$T_A = \text{Full range}$			2	nA
$I_{IB}$	Input bias current <sup>(3)</sup>	$V_O = 0$	$T_A = 25^\circ\text{C}$		65	200	pA
			$T_A = \text{Full range}$			7	nA
$V_{ICR}$	Common-mode input voltage range	$T_A = 25^\circ\text{C}$		$\pm 11$	–12 to 15		V
$V_{OM}$	Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$	$\pm 12$	$\pm 13.5$		V
		$R_L \geq 10\ \text{k}\Omega$	$T_A = \text{Full range}$	$\pm 12$			
		$R_L \geq 2\ \text{k}\Omega$		$\pm 10$			
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}$ $R_L \geq 2\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$	50	200		V/mV
			$T_A = \text{Full range}$	25			
$B_1$	Utility-gain bandwidth	$T_A = 25^\circ\text{C}$			3		MHz
$r_i$	Input resistance	$T_A = 25^\circ\text{C}$			$10^{12}$		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(\text{min})}$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	75	100		dB
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm} / \Delta V_{IO}$ )	$V_{CC} = \pm 9\ \text{V to } \pm 15\ \text{V}$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	80	100		dB
$I_{CC}$	Supply current (each amplifier)	$V_O = 0$ ; no load			1.4	2.5	mA
$V_{O1} / V_{O2}$	Crosstalk attenuation	$A_{VD} = 100$			120		dB

- (1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
- (2) Full range is  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ .
- (3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 1](#). Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

## 6.12 Electrical Characteristics: TL071BC, TL072BC, TL074BC

 $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup> <sup>(2)</sup>		MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		2	3	mV
			$T_A = \text{Full range}$			5	
$\alpha$	Temperature coefficient of input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = \text{Full range}$		18		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$	Input offset current	$V_O = 0$	$T_A = 25^\circ\text{C}$		5	100	pA
			$T_A = \text{Full range}$				2
$I_{IB}$	Input bias current <sup>(3)</sup>	$V_O = 0$	$T_A = 25^\circ\text{C}$		65	200	pA
			$T_A = \text{Full range}$				7
$V_{ICR}$	Common-mode input voltage range	$T_A = 25^\circ\text{C}$		$\pm 11$	–12 to 15		V
$V_{OM}$	Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$	$\pm 12$	$\pm 13.5$		V
		$R_L \geq 10\ \text{k}\Omega$	$T_A = \text{Full range}$	$\pm 12$			
		$R_L \geq 2\ \text{k}\Omega$		$\pm 10$			
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}$ $R_L \geq 2\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$	50	200		V/mV
			$T_A = \text{Full range}$	25			
$B_1$	Utility-gain bandwidth	$T_A = 25^\circ\text{C}$			3		MHz
$r_i$	Input resistance	$T_A = 25^\circ\text{C}$			$10^{12}$		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(\text{min})}$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	75	100		dB
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = \pm 9\ \text{V}$ to $\pm 15\ \text{V}$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	80	100		dB
$I_{CC}$	Supply current (each amplifier)	$V_O = 0$ ; no load		$T_A = 25^\circ\text{C}$	1.4	2.5	mA
$V_{O1} / V_{O2}$	Crosstalk attenuation	$A_{VD} = 100$		$T_A = 25^\circ\text{C}$	120		dB

- (1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
- (2) Full range is  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ .
- (3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 1](#). Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

### 6.13 Electrical Characteristics: TL071I, TL072I, TL074I

$V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		3	6	mV
			$T_A = \text{Full range}$			8	
$\alpha$	Temperature coefficient of input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = \text{Full range}$		18		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$	Input offset current	$V_O = 0$	$T_A = 25^\circ\text{C}$		5	100	pA
			$T_A = \text{Full range}$			2	nA
$I_{IB}$	Input bias current (3)	$V_O = 0$	$T_A = 25^\circ\text{C}$		65	200	pA
			$T_A = \text{Full range}$			7	nA
$V_{ICR}$	Common-mode input voltage range	$T_A = 25^\circ\text{C}$		$\pm 11$	–12 to 15		V
$V_{OM}$	Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$	$\pm 12$	$\pm 13.5$		V
		$R_L \geq 10\ \text{k}\Omega$	$T_A = \text{Full range}$	$\pm 12$			
		$R_L \geq 2\ \text{k}\Omega$		$\pm 10$			
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}$ $R_L \geq 2\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$	50	200		V/mV
			$T_A = \text{Full range}$	25			
$B_1$	Utility-gain bandwidth	$T_A = 25^\circ\text{C}$			3		MHz
$r_i$	Input resistance	$T_A = 25^\circ\text{C}$			$10^{12}$		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(\text{min})}$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	75	100		dB
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = \pm 9\ \text{V}$ to $\pm 15\ \text{V}$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	80	100		dB
$I_{CC}$	Supply current (each amplifier)	$V_O = 0$ ; no load			1.4	2.5	mA
$V_{O1} / V_{O2}$	Crosstalk attenuation	$A_{VD} = 100$			120		dB

- (1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
- (2)  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .
- (3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 1. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.



## 6.14 Electrical Characteristics: TL071M, TL072M

 $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup> <sup>(2)</sup>		MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		3	6	mV
			$T_A = \text{Full range}$			9	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = \text{Full range}$		18		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$	Input offset current	$V_O = 0$	$T_A = 25^\circ\text{C}$		5	100	pA
			$T_A = \text{Full range}$			20	nA
$I_{IB}$	Input bias current	$V_O = 0$	$T_A = 25^\circ\text{C}$		65	200	pA
			$T_A = \text{Full range}$			50	nA
$V_{ICR}$	Common-mode input voltage range	$T_A = 25^\circ\text{C}$		$\pm 11$	–12 to 15		V
$V_{OM}$	Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$	$\pm 12$	$\pm 13.5$		V
		$R_L \geq 10\ \text{k}\Omega$	$T_A = \text{Full range}$	$\pm 12$			
		$R_L \geq 2\ \text{k}\Omega$		$\pm 10$			
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}$ $R_L \geq 2\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$	35	200		V/mV
			$T_A = \text{Full range}$	15			
$B_1$	Unity-gain bandwidth				3		MHz
$r_i$	Input resistance				$10^{12}$		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(\text{min})}$ , $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	80	86		dB
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = \pm 9\ \text{V}$ to $\pm 15\ \text{V}$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	80	86		dB
$I_{CC}$	Supply current (each amplifier)	$V_O = 0$ ; no load	$T_A = 25^\circ\text{C}$		1.4	2.5	mA
$V_{O1} / V_{O2}$	Crosstalk attenuation	$A_{VD} = 100$			120		dB

- Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 1](#). Pulse techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.
- All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

## 6.15 Electrical Characteristics: TL074M

$V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		3	9	mV
			$T_A = \text{Full range}$			15	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_O = 0, R_S = 50\ \Omega$	$T_A = \text{Full range}$		18		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$	Input offset current	$V_O = 0$	$T_A = 25^\circ\text{C}$		5	100	pA
			$T_A = \text{Full range}$			20	nA
$I_{IB}$	Input bias current	$V_O = 0$	$T_A = 25^\circ\text{C}$		65	200	pA
			$T_A = \text{Full range}$			20	nA
$V_{ICR}$	Common-mode input voltage range	$T_A = 25^\circ\text{C}$		$\pm 11$	–12 to 15		V
$V_{OM}$	Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$	$\pm 12$	$\pm 13.5$		V
		$R_L \geq 10\ \text{k}\Omega$	$T_A = \text{Full range}$	$\pm 12$			
		$R_L \geq 2\ \text{k}\Omega$		$\pm 10$			
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}$ $R_L \geq 2\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$	35	200		V/mV
			$T_A = \text{Full range}$	15			
$B_1$	Unity-gain bandwidth				3		MHz
$r_i$	Input resistance				$10^{12}$		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(\text{min})}$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	80	86		dB
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = \pm 9\ \text{V to } \pm 15\ \text{V}$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	80	86		dB
$I_{CC}$	Supply current (each amplifier)	$V_O = 0$ ; no load	$T_A = 25^\circ\text{C}$		1.4	2.5	mA
$V_{O1} / V_{O2}$	Crosstalk attenuation	$A_{VD} = 100$	$T_A = 25^\circ\text{C}$		120		dB

- (1) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 1. Pulse techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.
- (2) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

### 6.16 Switching Characteristics: TL07xM

 $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10\text{ V}$ $C_L = 100\text{ pF}$	$R_L = 2\text{ k}\Omega$ See <a href="#">Figure 21</a>	5	13		V/ $\mu\text{s}$
$t_r$	Rise-time overshoot factor	$V_I = 20\text{ V}$ $C_L = 100\text{ pF}$	$R_L = 2\text{ k}\Omega$ See <a href="#">Figure 21</a>		0.1		$\mu\text{s}$
					20%		
$V_n$	Equivalent input noise voltage	$R_S = 20\ \Omega$	$f = 1\text{ kHz}$		18		nV/ $\sqrt{\text{Hz}}$
			$f = 10\text{ Hz to } 10\text{ kHz}$		4		$\mu\text{V}$
$I_n$	Equivalent input noise current	$R_S = 20\ \Omega$	$f = 1\text{ kHz}$		0.01		pA/ $\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$V_{\text{rms}} = 6\text{ V}$ $R_L \geq 2\text{ k}\Omega$ $f = 1\text{ kHz}$	$A_{\text{VD}} = 1$ $R_S \leq 1\text{ k}\Omega$		0.003%		

### 6.17 Switching Characteristics: TL07xC, TL07xAC, TL07xBC, TL07xI

 $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10\text{ V}$ $C_L = 100\text{ pF}$	$R_L = 2\text{ k}\Omega$ See <a href="#">Figure 21</a>	8	13		V/ $\mu\text{s}$
$t_r$	Rise-time overshoot factor	$V_I = 20\text{ V}$ $C_L = 100\text{ pF}$	$R_L = 2\text{ k}\Omega$ See <a href="#">Figure 21</a>		0.1		$\mu\text{s}$
					20%		
$V_n$	Equivalent input noise voltage	$R_S = 20\ \Omega$	$f = 1\text{ kHz}$		18		nV/ $\sqrt{\text{Hz}}$
			$f = 10\text{ Hz to } 10\text{ kHz}$		4		$\mu\text{V}$
$I_n$	Equivalent input noise current	$R_S = 20\ \Omega$	$f = 1\text{ kHz}$		0.01		pA/ $\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$V_{\text{rms}} = 6\text{ V}$ $R_L \geq 2\text{ k}\Omega$ $f = 1\text{ kHz}$	$A_{\text{VD}} = 1$ $R_S \leq 1\text{ k}\Omega$		0.003%		

## 6.18 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**Table 1. Typical Characteristics: Table of Graphs**

			FIGURE
$I_{IB}$	Input bias current	versus free-air temperature	<a href="#">Figure 1</a>
$V_{OM}$	Maximum peak output voltage	versus frequency	<a href="#">Figure 2</a>
			<a href="#">Figure 3</a>
			<a href="#">Figure 4</a>
		versus free-air temperature	<a href="#">Figure 5</a>
		versus load resistance	<a href="#">Figure 6</a>
	versus supply voltage	<a href="#">Figure 7</a>	
$A_{VD}$	Large signal differential voltage amplification	versus free-air temperature	<a href="#">Figure 8</a>
		versus load resistance	<a href="#">Figure 9</a>
	Phase shift	versus frequency	<a href="#">Figure 9</a>
	Normalized unity-gain bandwidth	versus free-air temperature	<a href="#">Figure 10</a>
	Normalized phase shift	versus free-air temperature	<a href="#">Figure 10</a>
CMRR	Common-mode rejection ratio	versus free-air temperature	<a href="#">Figure 11</a>
	Input offset voltage change	versus common-mode voltage	<a href="#">Figure 20</a>
$I_{CC}$	Supply current	versus free-air temperature	<a href="#">Figure 13</a>
		versus supply voltage	<a href="#">Figure 12</a>
$P_D$	Total power dissipation	versus free-air temperature	<a href="#">Figure 14</a>
	Normalized slew rate	versus free-air temperature	<a href="#">Figure 15</a>
$V_n$	Equivalent input noise voltage	versus frequency	<a href="#">Figure 16</a>
THD	Total harmonic distortion	versus frequency	<a href="#">Figure 17</a>
	Large-signal pulse response	versus time	<a href="#">Figure 18</a>
$V_O$	Output voltage	versus elapsed time	<a href="#">Figure 19</a>

6.18.1 Typical Characteristics

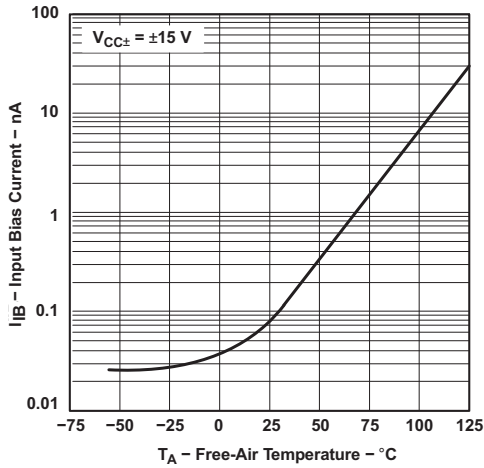


Figure 1. Input Bias Current vs Free-Air Temperature

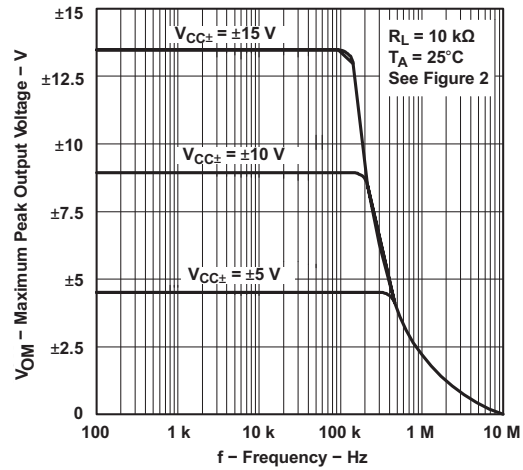


Figure 2. Maximum Peak Output Voltage vs Frequency

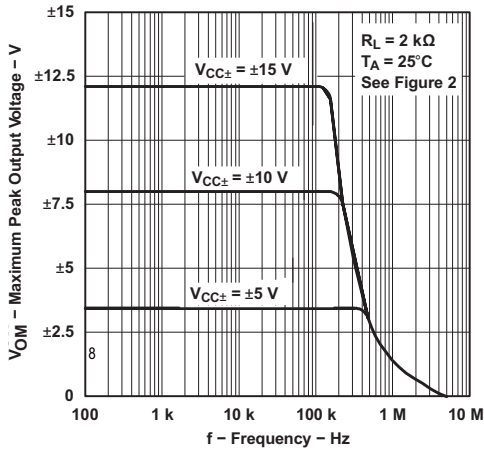


Figure 3. Maximum Peak Output Voltage vs Frequency

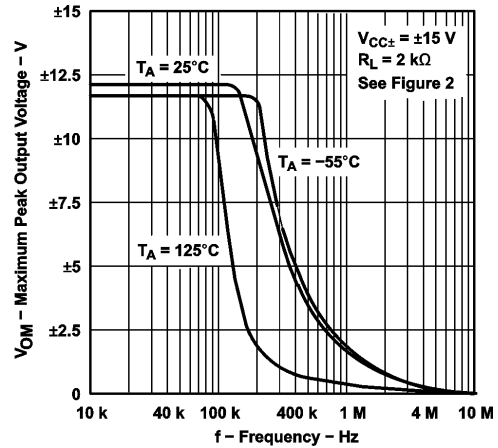


Figure 4. Maximum Peak Output Voltage vs Frequency

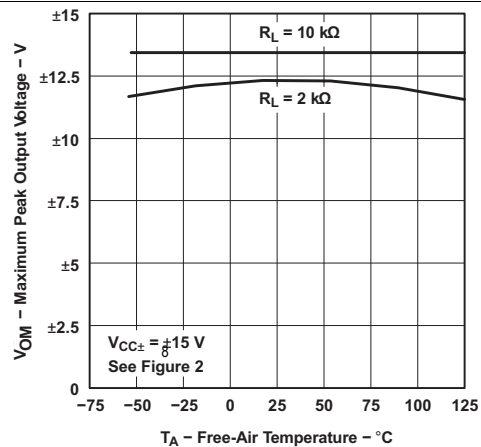


Figure 5. Maximum Peak Output Voltage vs Free-Air Temperature

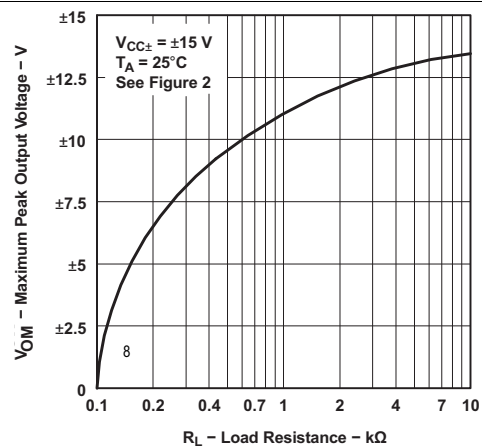


Figure 6. Maximum Peak Output Voltage vs Load Resistance

Typical Characteristics (continued)

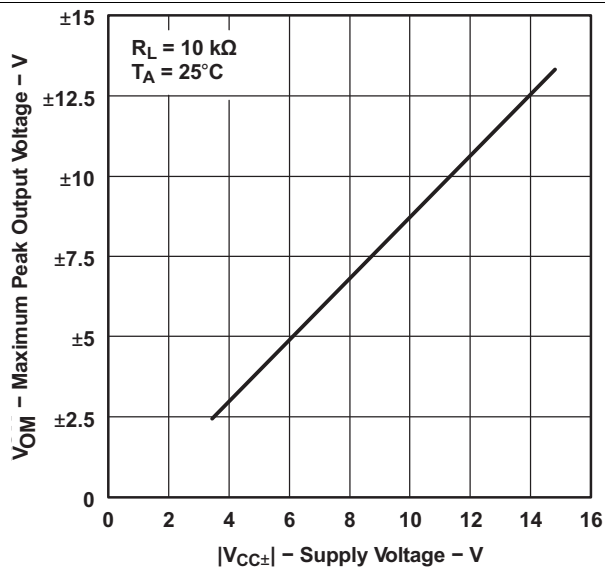


Figure 7. Maximum Peak Output Voltage vs Supply Voltage

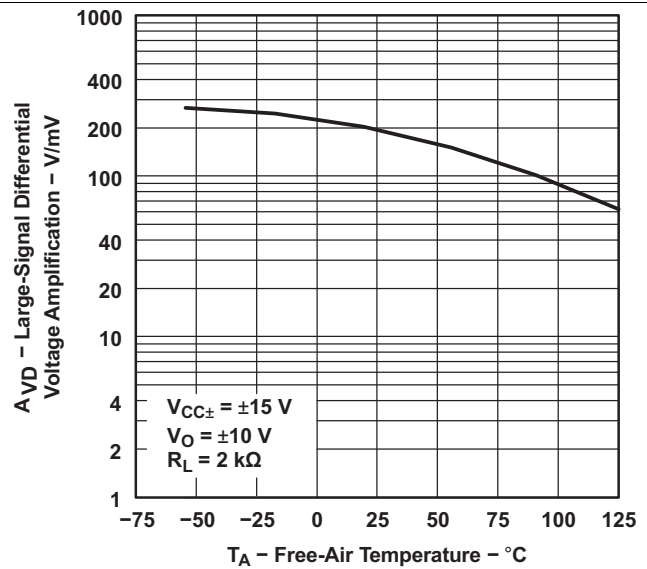


Figure 8. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

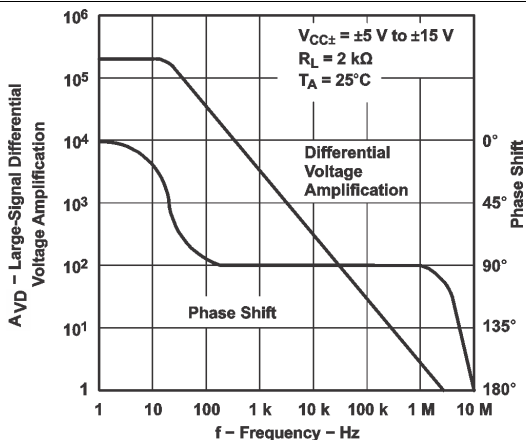


Figure 9. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

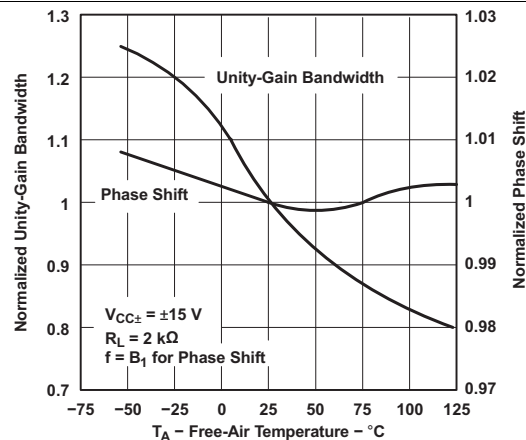


Figure 10. Normalized Unity-Gain Bandwidth and Phase Shift vs Free-Air Temperature

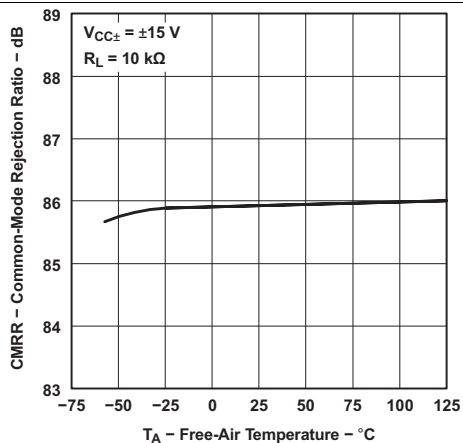


Figure 11. Common-Mode Rejection Ratio vs Free-Air Temperature

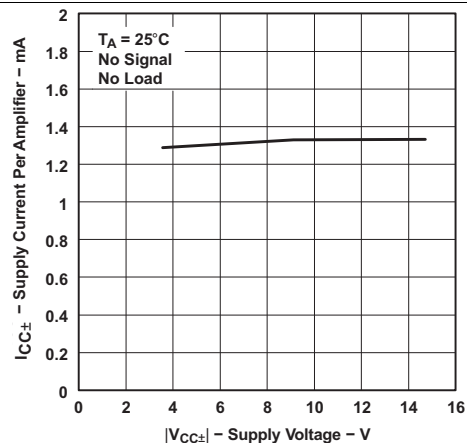


Figure 12. Supply Current Per Amplifier vs Supply Voltage

Typical Characteristics (continued)

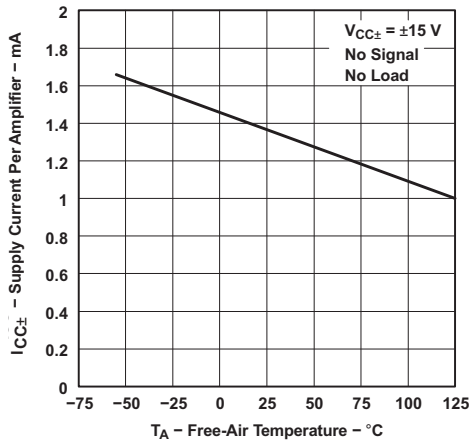


Figure 13. Supply Current Per Amplifier vs Free-Air Temperature

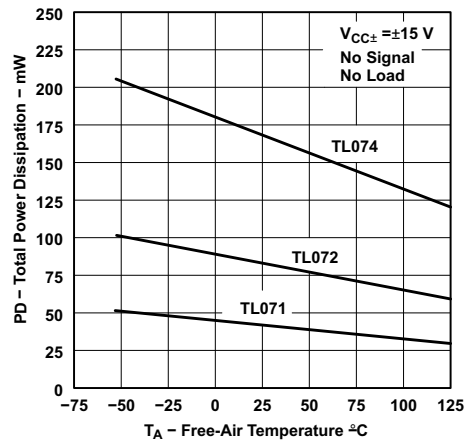


Figure 14. Total Power Dissipation vs Free-Air Temperature

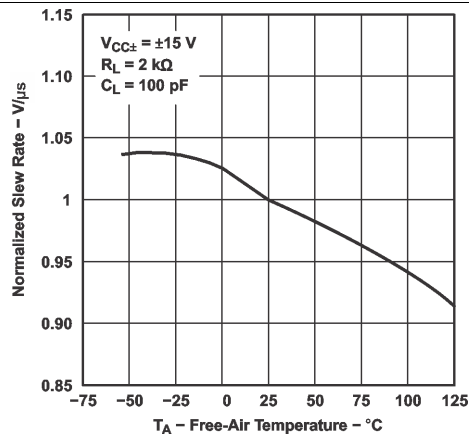


Figure 15. Normalized Slew Rate vs Free-Air Temperature

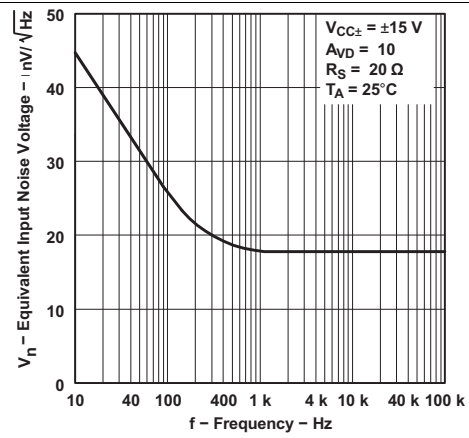


Figure 16. Equivalent Input Noise Voltage vs Frequency

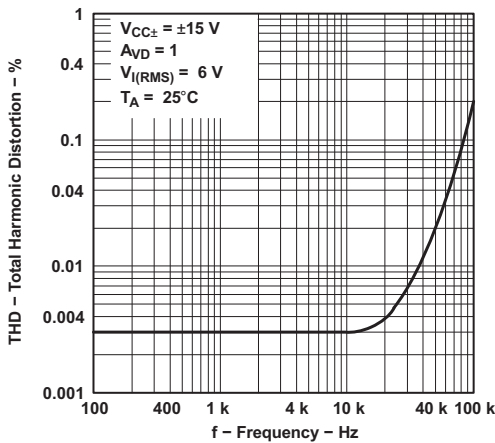


Figure 17. Total Harmonic Distortion vs Frequency

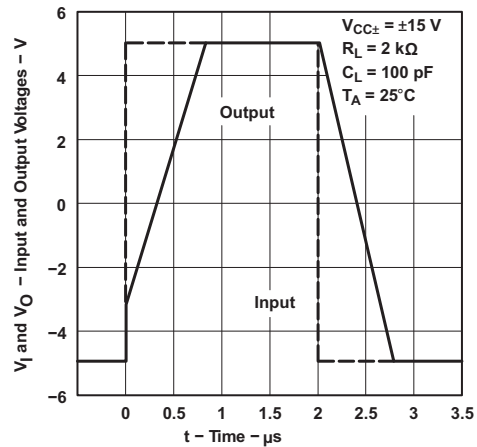
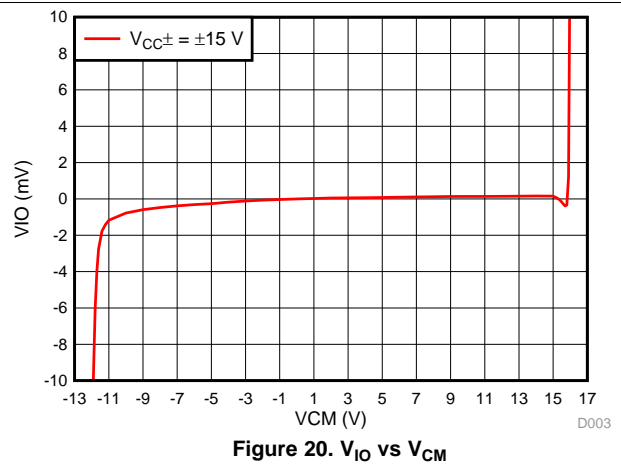
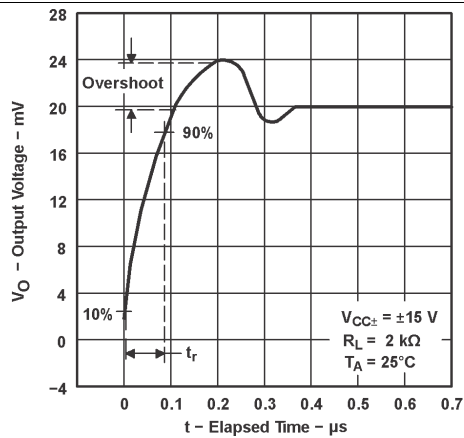


Figure 18. Voltage-Follower Large-Signal Pulse Response

Typical Characteristics (continued)





## 6.1 Parameter Measurement Information

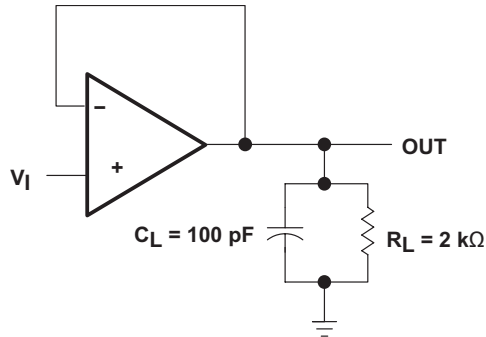


Figure 21. Unity-Gain Amplifier

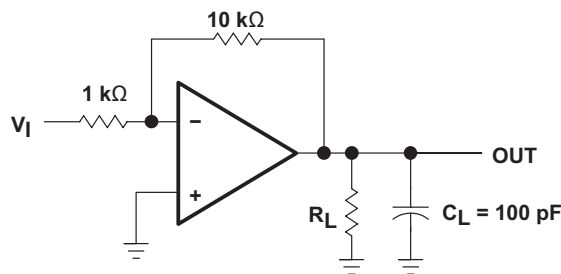


Figure 22. Gain-of-10 Inverting Amplifier

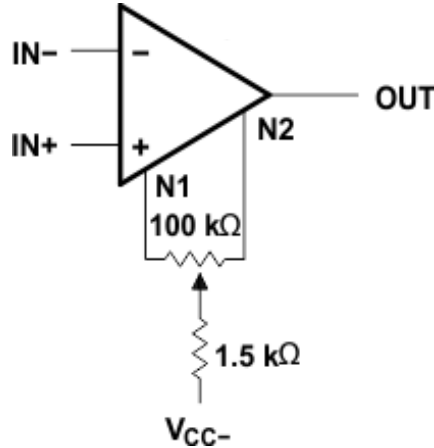


Figure 23. Input Offset-Voltage Null Circuit

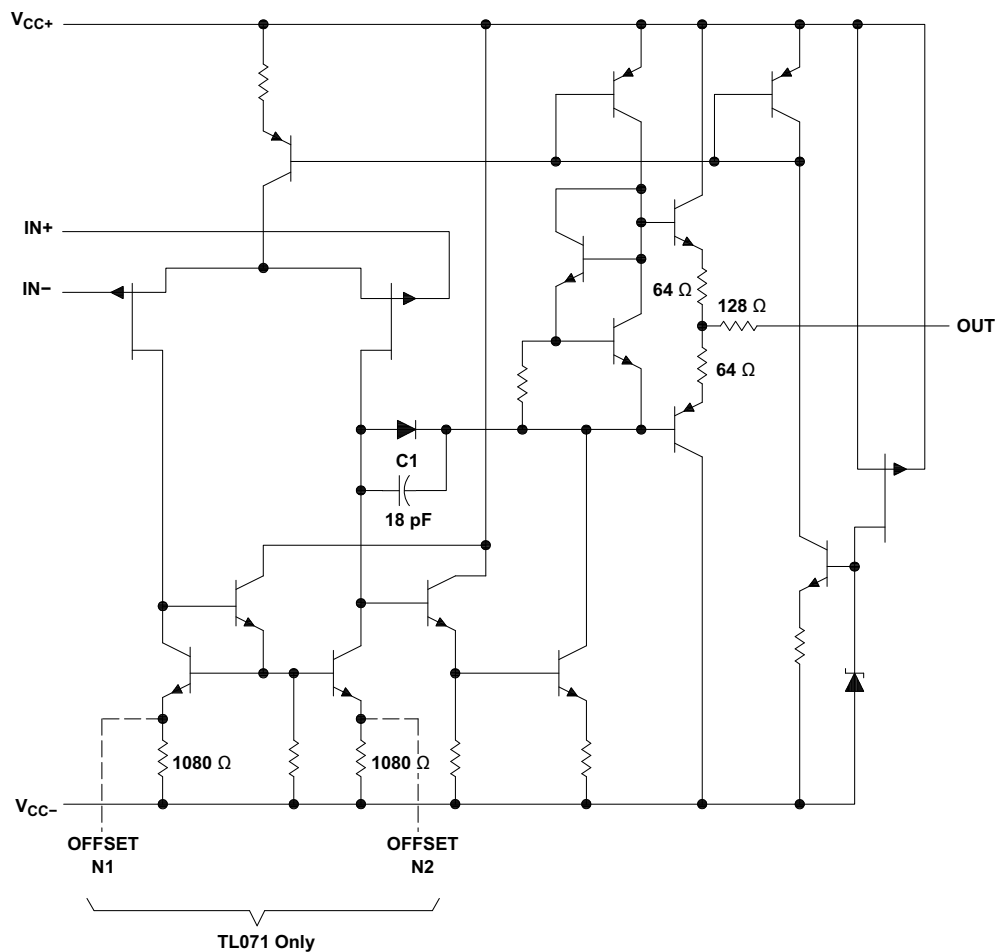
## 7 Detailed Description

### 7.1 Overview

The JFET-input operational amplifiers in the TL07xx series are similar to the TL08x series, with low input bias and offset currents, and a fast slew rate. The low harmonic distortion and low noise make the TL07xx series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from -40°C to +85°C. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to +125°C.

### 7.2 Functional Block Diagram



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

## 7.3 Feature Description

### 7.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL07x device adds little harmonic distortion when used in audio signal applications.

### 7.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change the output when there is a change on the input. These devices have a 13-V/ $\mu$ s slew rate.

## 7.4 Device Functional Modes

These devices are powered on when the supply is connected. These devices can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

## 8 Application and Implementation

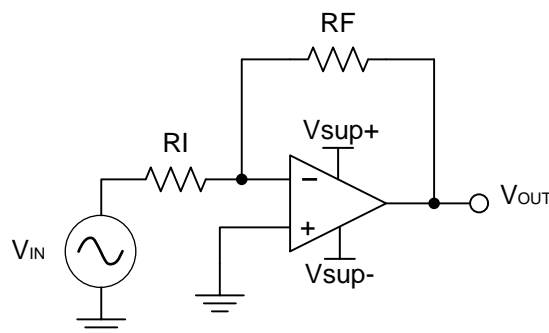
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes the voltage a negative voltage. In the same manner, the amplifier makes negative voltages positive.

### 8.2 Typical Application



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**Figure 24. Inverting Amplifier**

#### 8.2.1 Design Requirements

The supply voltage must be selected so the supply voltage is larger than the input voltage range and output range. For instance, this application scales a signal of  $\pm 0.5$  V to  $\pm 1.8$  V. Setting the supply at  $\pm 12$  V is sufficient to accommodate this application.

#### 8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_v = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, select a value for  $R_I$  or  $R_F$ . Selecting a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliamp range. This ensures the part does not draw too much current. This example uses  $10 \text{ k}\Omega$  for  $R_I$  which means  $36 \text{ k}\Omega$  is used for  $R_F$ . This is determined by [Equation 3](#).

$$A_v = -\frac{R_F}{R_I} \quad (3)$$

## Typical Application (continued)

### 8.2.3 Application Curve

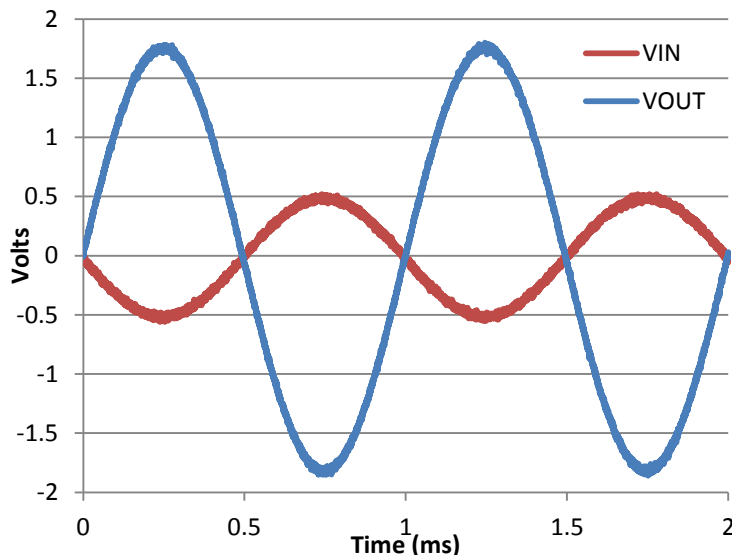
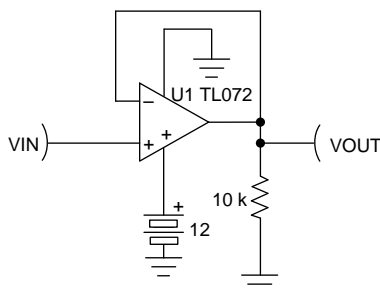


Figure 25. Input and Output Voltages of the Inverting Amplifier

## 8.3 Unity Gain Buffer



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Figure 26. Single-Supply Unity Gain Amplifier

### 8.3.1 Design Requirements

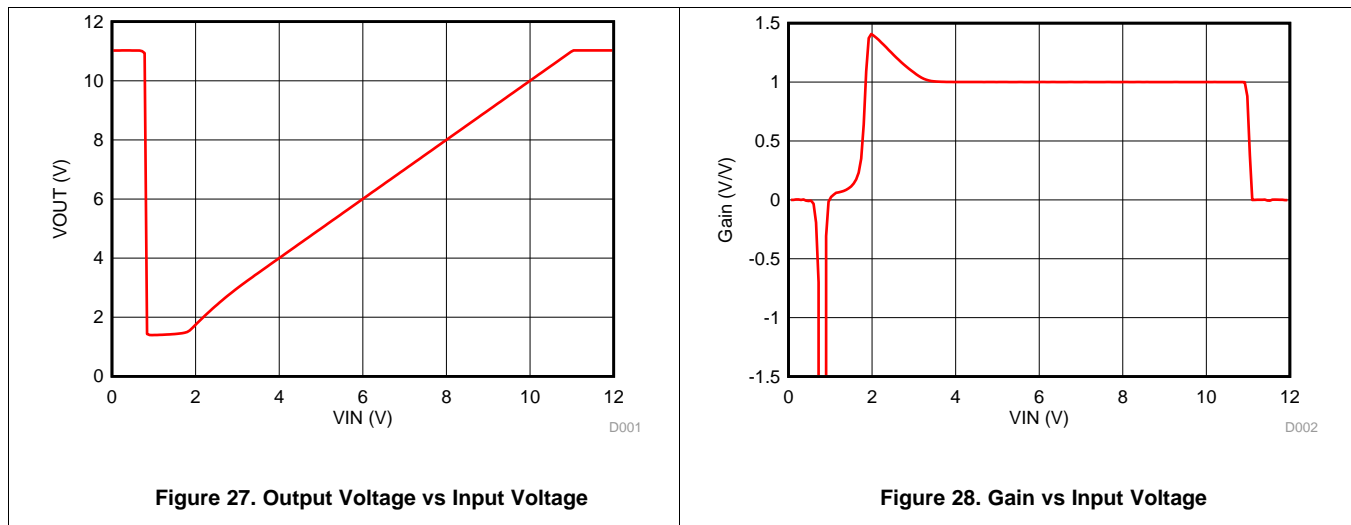
- $V_{CC}$  must be within valid range per [Recommended Operating Conditions](#). This example uses a value of 12 V for  $V_{CC}$ .
- Input voltage must be within the recommended common-mode range, as shown in [Recommended Operating Conditions](#). The valid common-mode range is 4 V to 12 V ( $V_{CC-} + 4$  V to  $V_{CC+}$ ).
- Output is limited by output range, which is typically 1.5 V to 10.5 V, or  $V_{CC-} + 1.5$  V to  $V_{CC+} - 1.5$  V.

### 8.3.2 Detailed Design Procedure

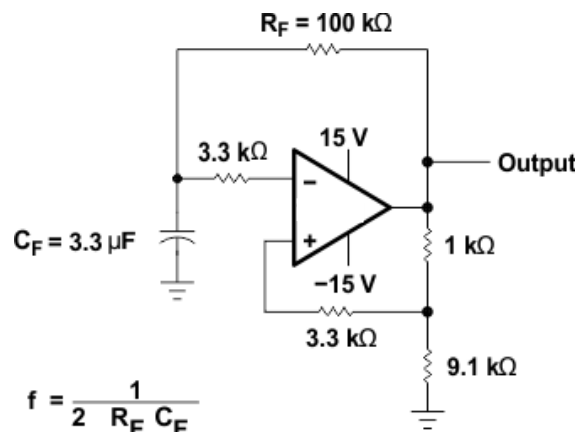
- Avoid input voltage values below 1 V to prevent phase reversal where output goes high.
- Avoid input values below 4 V to prevent degraded  $V_{IO}$  that results in an apparent gain greater than 1. This may cause instability in some second-order filter designs.

## Unity Gain Buffer (continued)

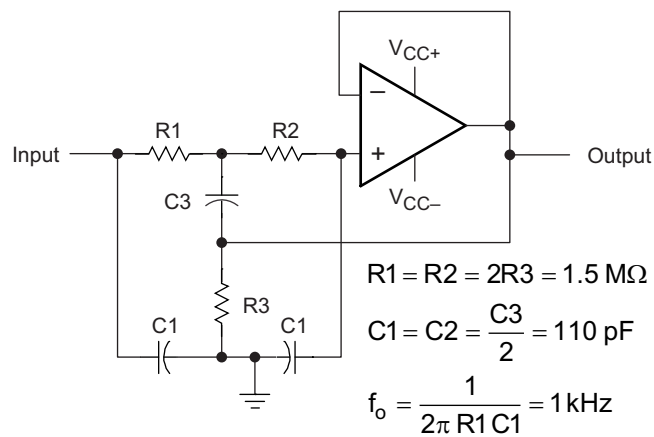
### 8.3.3 Application Curves



### 8.4 System Examples



**Figure 29. 0.5-Hz Square-Wave Oscillator**



**Figure 30. High-Q Notch Filter**

System Examples (continued)

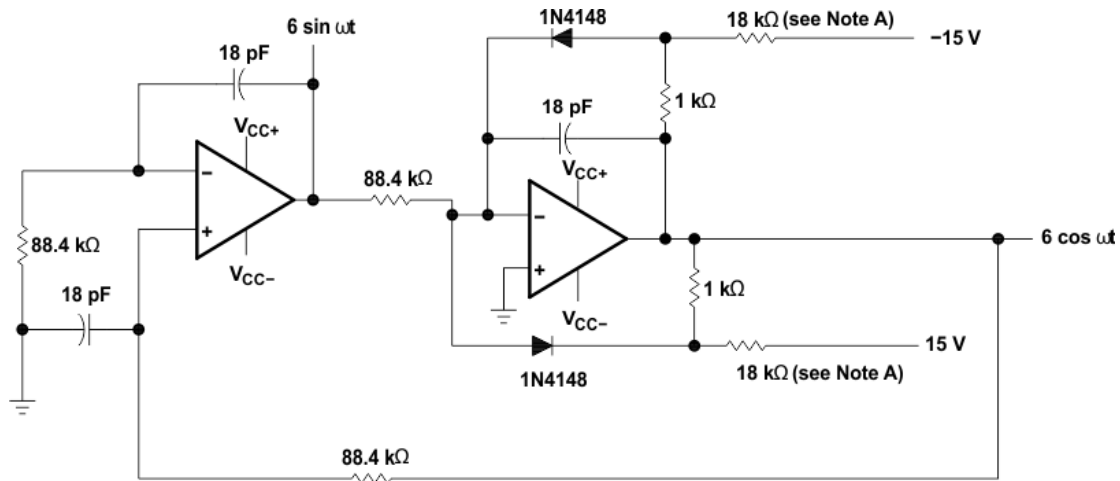


Figure 31. 100-kHz Quadrature Oscillator

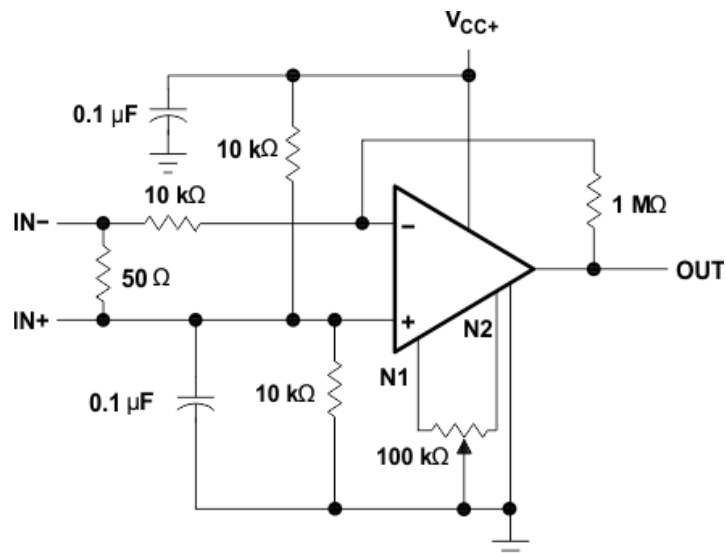


Figure 32. AC Amplifier

## 9 Power Supply Recommendations

### CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of  $\pm 18$  V for a dual-supply can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- $\mu$ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Layout](#).

## 10 Layout

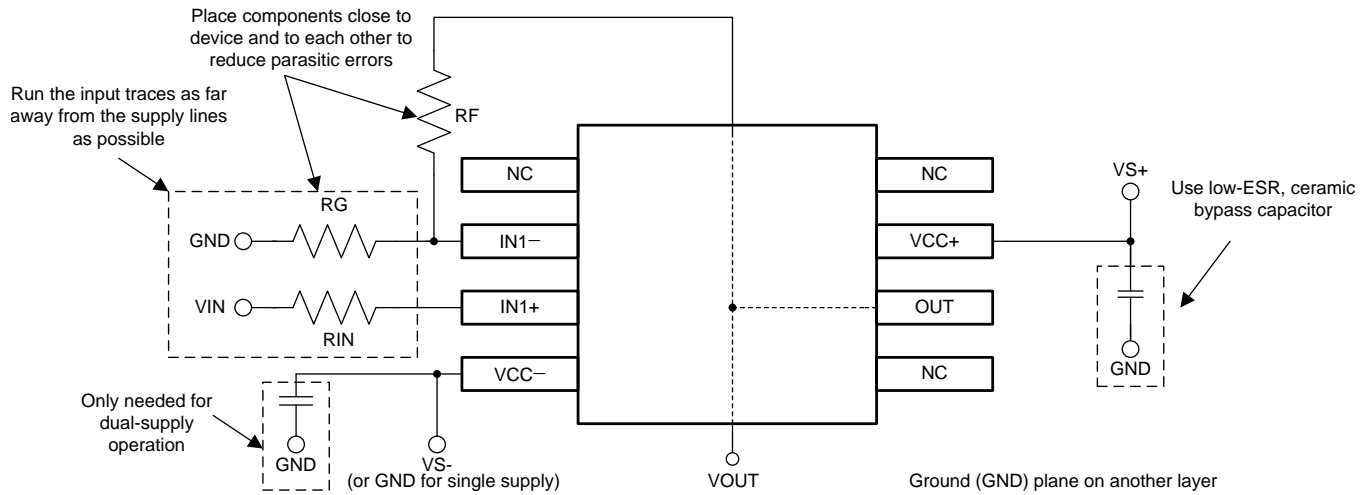
### 10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

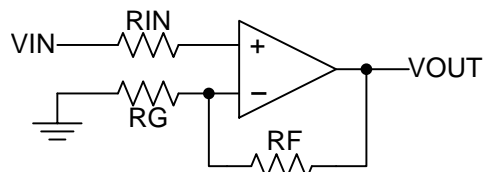
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Circuit Board Layout Techniques](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Example](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.



## 10.2 Layout Example



**Figure 33. Operational Amplifier Board Layout for Noninverting Configuration**



**Figure 34. Operational Amplifier Schematic for Noninverting Configuration**

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation, see the following:

[Circuit Board Layout Techniques](#) (SLOA089)

### 11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL071	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL071A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL071B	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL072	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL072A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL072B	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL072M	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL074	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL074A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL074B	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL074M	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.  
 All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
81023052A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	<a href="#">Samples</a>
8102305HA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102305HA TL072M	<a href="#">Samples</a>
8102305PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102305PA TL072M	<a href="#">Samples</a>
81023062A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	<a href="#">Samples</a>
8102306CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	<a href="#">Samples</a>
8102306DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	<a href="#">Samples</a>
JM38510/11905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	<a href="#">Samples</a>
M38510/11905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	<a href="#">Samples</a>
TL071ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	<a href="#">Samples</a>
TL071ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	<a href="#">Samples</a>
TL071ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	<a href="#">Samples</a>
TL071ACP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071ACP	<a href="#">Samples</a>
TL071BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	<a href="#">Samples</a>
TL071BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	<a href="#">Samples</a>
TL071BCP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071BCP	<a href="#">Samples</a>
TL071CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	<a href="#">Samples</a>
TL071CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL071CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	<a href="#">Samples</a>
TL071CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	<a href="#">Samples</a>
TL071CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071CP	<a href="#">Samples</a>
TL071CPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071CP	<a href="#">Samples</a>
TL071CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T071	<a href="#">Samples</a>
TL071ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	<a href="#">Samples</a>
TL071IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	<a href="#">Samples</a>
TL071IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	<a href="#">Samples</a>
TL071IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL071IP	<a href="#">Samples</a>
TL072ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	<a href="#">Samples</a>
TL072ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	<a href="#">Samples</a>
TL072ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	<a href="#">Samples</a>
TL072ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	<a href="#">Samples</a>
TL072ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	<a href="#">Samples</a>
TL072ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP	<a href="#">Samples</a>
TL072ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP	<a href="#">Samples</a>
TL072BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	<a href="#">Samples</a>
TL072BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	<a href="#">Samples</a>
TL072BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	<a href="#">Samples</a>
TL072BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	<a href="#">Samples</a>
TL072BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072BCP	<a href="#">Samples</a>
TL072BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072BCP	<a href="#">Samples</a>
TL072CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	<a href="#">Samples</a>
TL072CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	<a href="#">Samples</a>
TL072CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	<a href="#">Samples</a>
TL072CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	<a href="#">Samples</a>
TL072CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	<a href="#">Samples</a>
TL072CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	<a href="#">Samples</a>
TL072CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072CP	<a href="#">Samples</a>
TL072CPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072CP	<a href="#">Samples</a>
TL072CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	<a href="#">Samples</a>
TL072CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	<a href="#">Samples</a>
TL072CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	<a href="#">Samples</a>
TL072CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	<a href="#">Samples</a>
TL072CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	<a href="#">Samples</a>
TL072ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	<a href="#">Samples</a>
TL072IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	<a href="#">Samples</a>
TL072IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	<a href="#">Samples</a>
TL072IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	<a href="#">Samples</a>
TL072IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	<a href="#">Samples</a>
TL072IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	<a href="#">Samples</a>
TL072IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL072IP	<a href="#">Samples</a>
TL072IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL072IP	<a href="#">Samples</a>
TL072MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	<a href="#">Samples</a>
TL072MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL072MJG	<a href="#">Samples</a>
TL072MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102305PA TL072M	<a href="#">Samples</a>
TL072MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102305HA TL072M	<a href="#">Samples</a>
TL074ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	<a href="#">Samples</a>
TL074ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	<a href="#">Samples</a>
TL074ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	<a href="#">Samples</a>
TL074ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	<a href="#">Samples</a>
TL074ACDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074ACN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN	<a href="#">Samples</a>
TL074ACNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN	<a href="#">Samples</a>
TL074ACNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A	<a href="#">Samples</a>
TL074BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	<a href="#">Samples</a>
TL074BCDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	<a href="#">Samples</a>
TL074BCDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	<a href="#">Samples</a>
TL074BCDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	<a href="#">Samples</a>
TL074BCDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	<a href="#">Samples</a>
TL074BCN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN	<a href="#">Samples</a>
TL074BCNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN	<a href="#">Samples</a>
TL074CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	<a href="#">Samples</a>
TL074CDBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	<a href="#">Samples</a>
TL074CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	<a href="#">Samples</a>
TL074CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	TL074C	<a href="#">Samples</a>
TL074CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	<a href="#">Samples</a>
TL074CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074CN	<a href="#">Samples</a>
TL074CNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074CN	<a href="#">Samples</a>
TL074CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074	<a href="#">Samples</a>
TL074CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	<a href="#">Samples</a>
TL074CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	<a href="#">Samples</a>
TL074CPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	<a href="#">Samples</a>
TL074CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	<a href="#">Samples</a>
TL074ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	<a href="#">Samples</a>
TL074IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	<a href="#">Samples</a>
TL074IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	<a href="#">Samples</a>
TL074IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	<a href="#">Samples</a>
TL074IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	<a href="#">Samples</a>
TL074IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	<a href="#">Samples</a>
TL074IN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL074IN	<a href="#">Samples</a>
TL074MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	TL074MFK	<a href="#">Samples</a>
TL074MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	<a href="#">Samples</a>
TL074MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL074MJ	<a href="#">Samples</a>
TL074MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	<a href="#">Samples</a>
TL074MWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TL072, TL072M, TL074, TL074M :**

● Catalog: [TL072](#), [TL074](#)

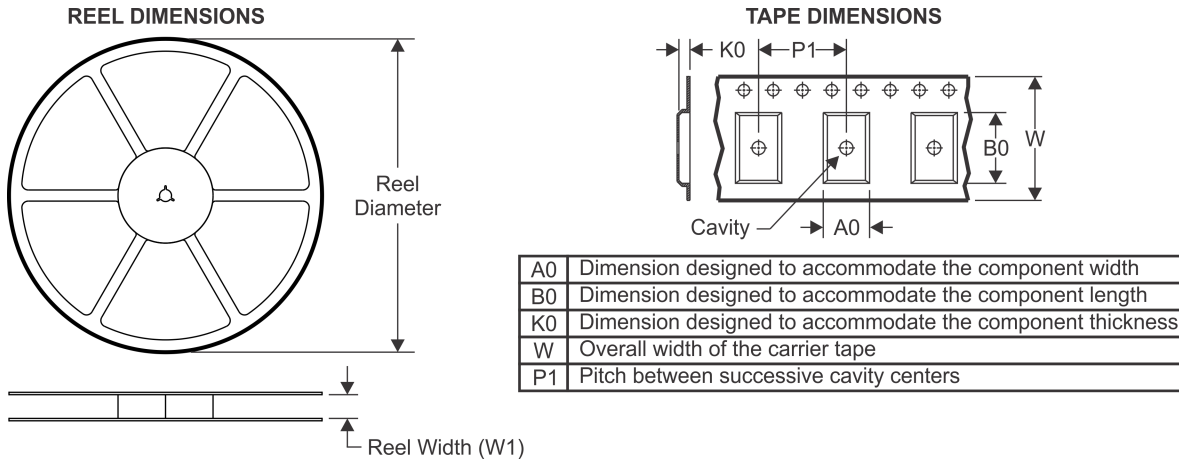
● Enhanced Product: [TL072-EP](#), [TL072-EP](#), [TL074-EP](#), [TL074-EP](#)

● Military: [TL072M](#), [TL074M](#)

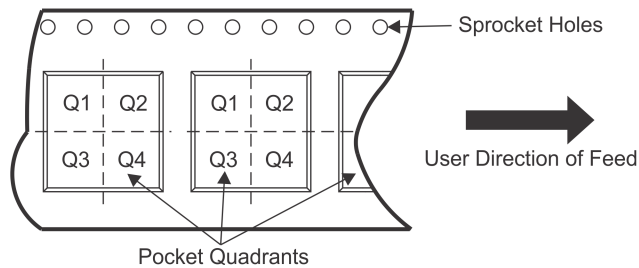
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

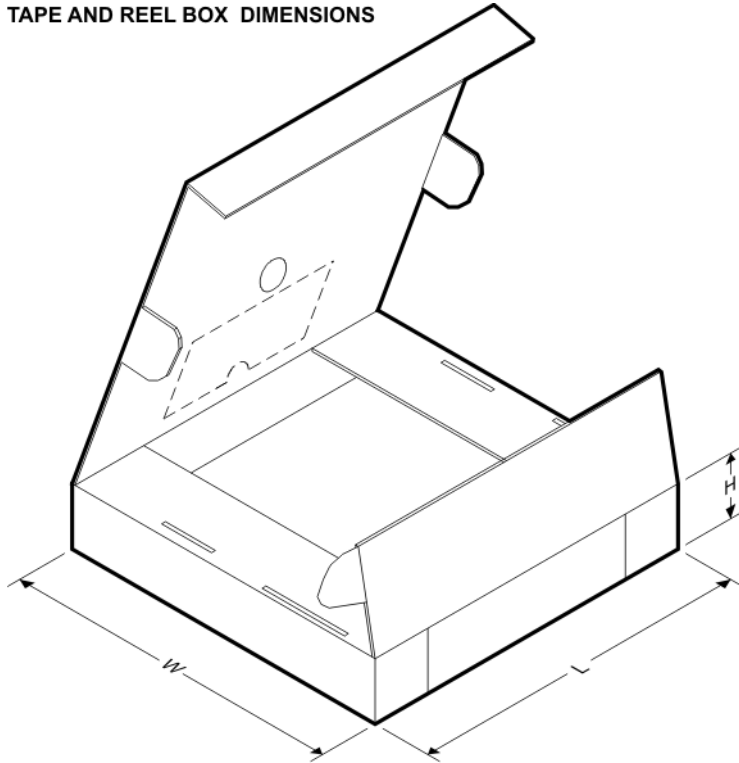


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL071ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL074ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL074IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL071ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL071IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL072CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL072IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL072IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL074ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TL074ACNSR	SO	NS	14	2000	367.0	367.0	38.0
TL074BCDR	SOIC	D	14	2500	333.2	345.9	28.6
TL074CDR	SOIC	D	14	2500	333.2	345.9	28.6

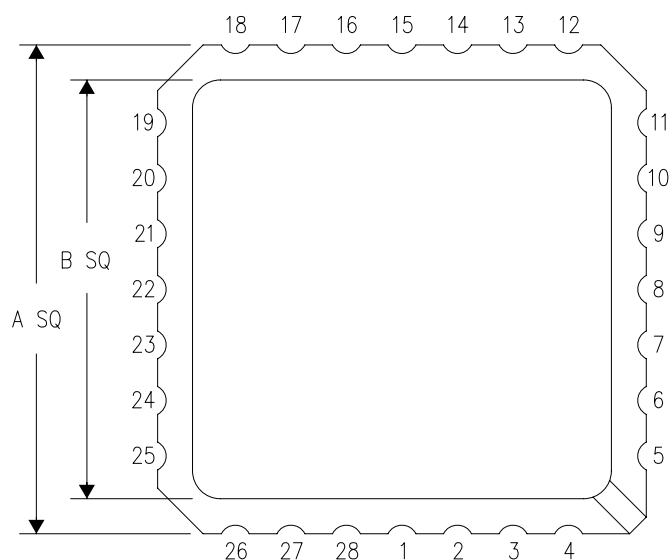
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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL074CDRG4	SOIC	D	14	2500	333.2	345.9	28.6
TL074CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TL074IDR	SOIC	D	14	2500	333.2	345.9	28.6

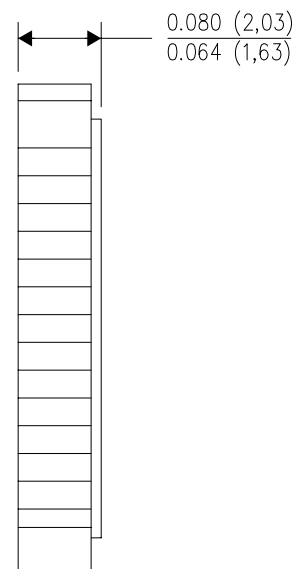
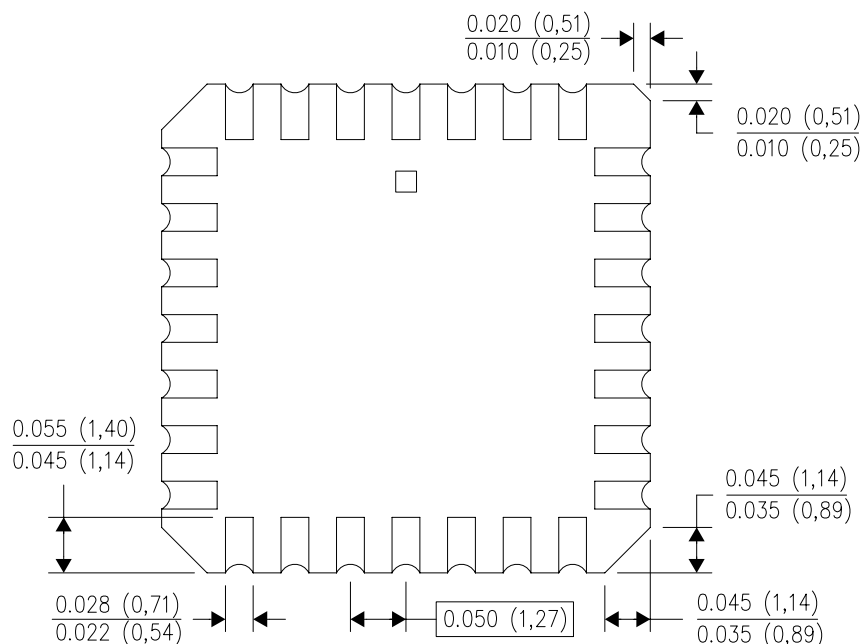
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

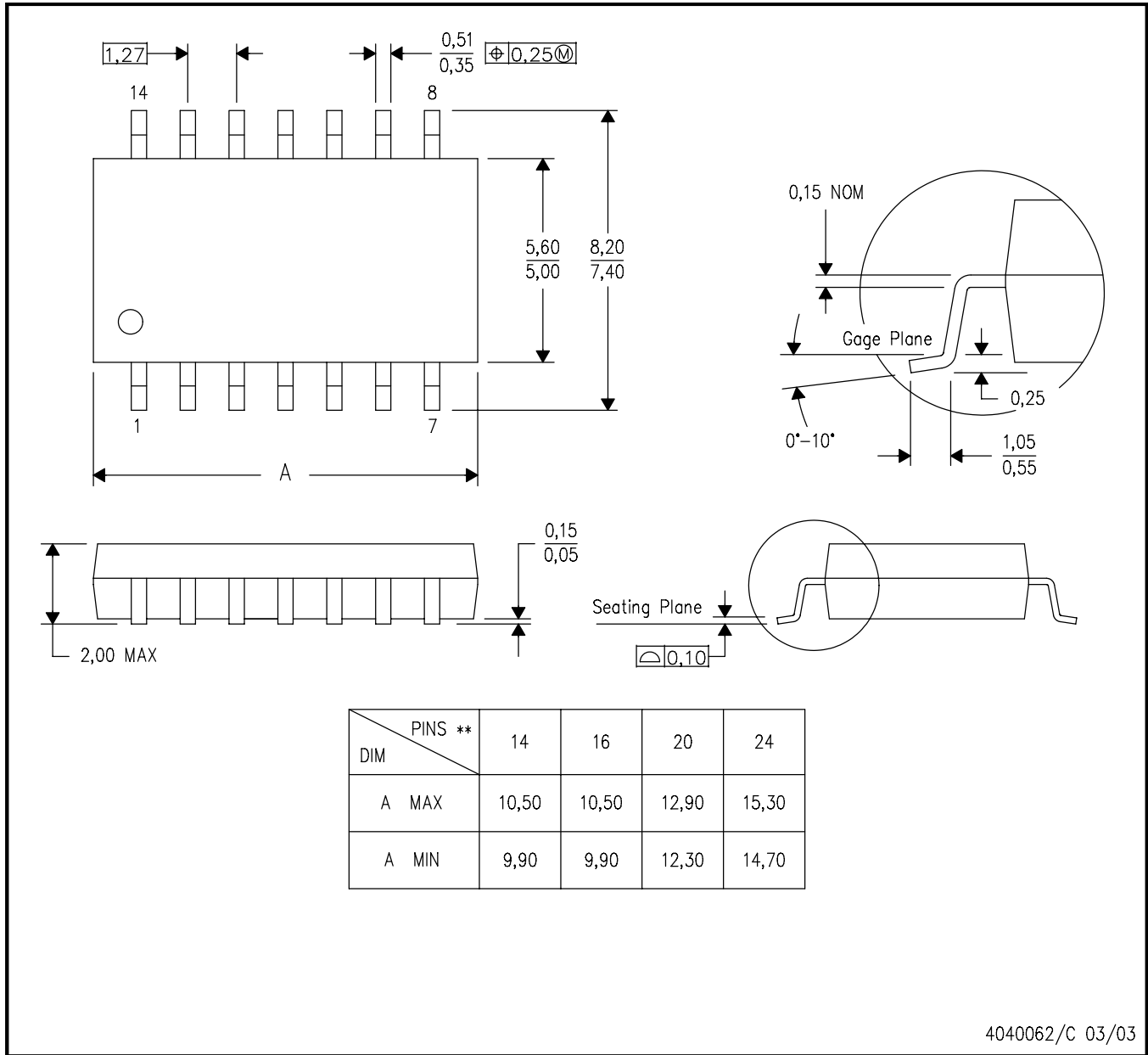
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

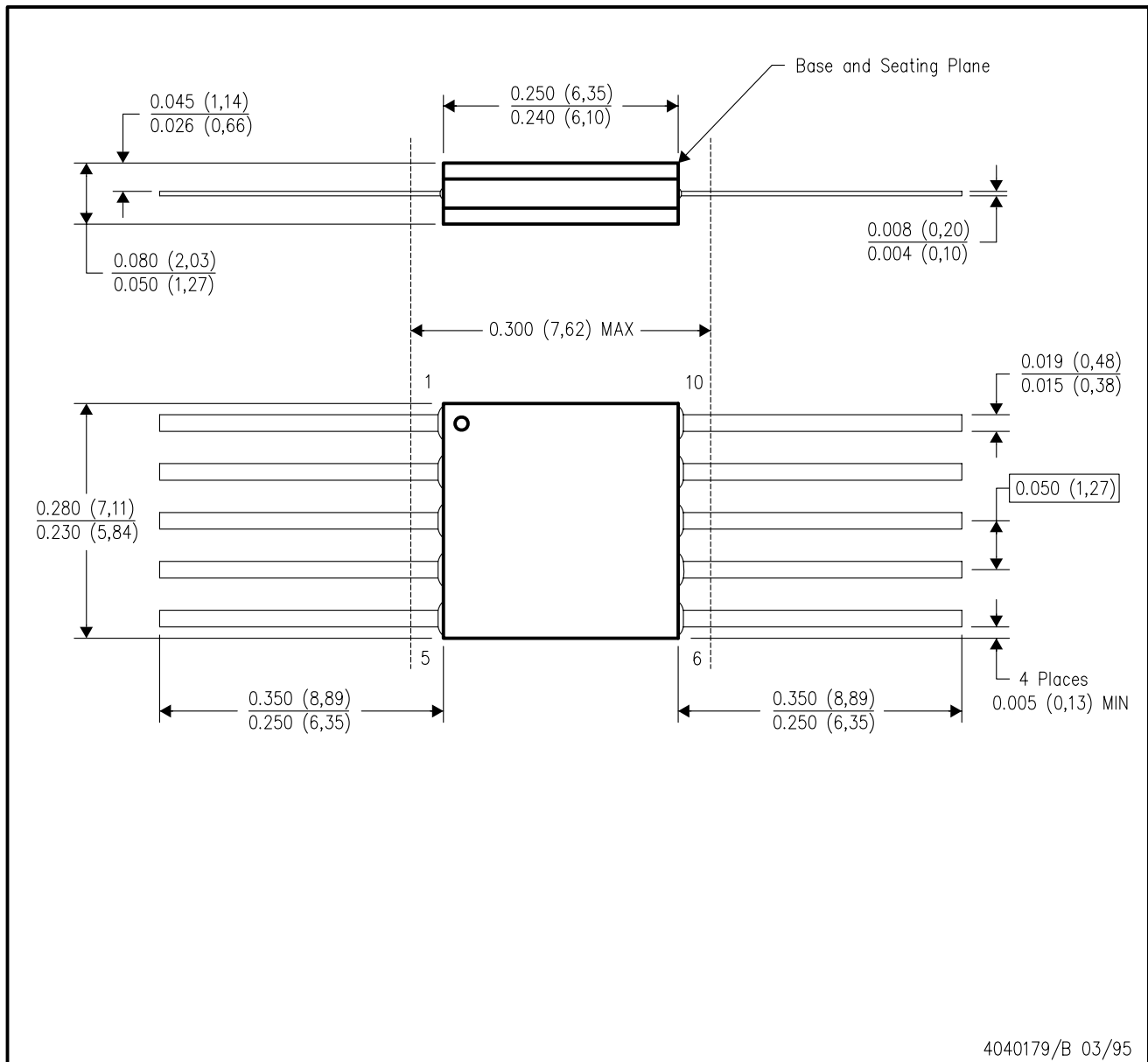


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



U (S-GDFP-F10)

CERAMIC DUAL FLATPACK

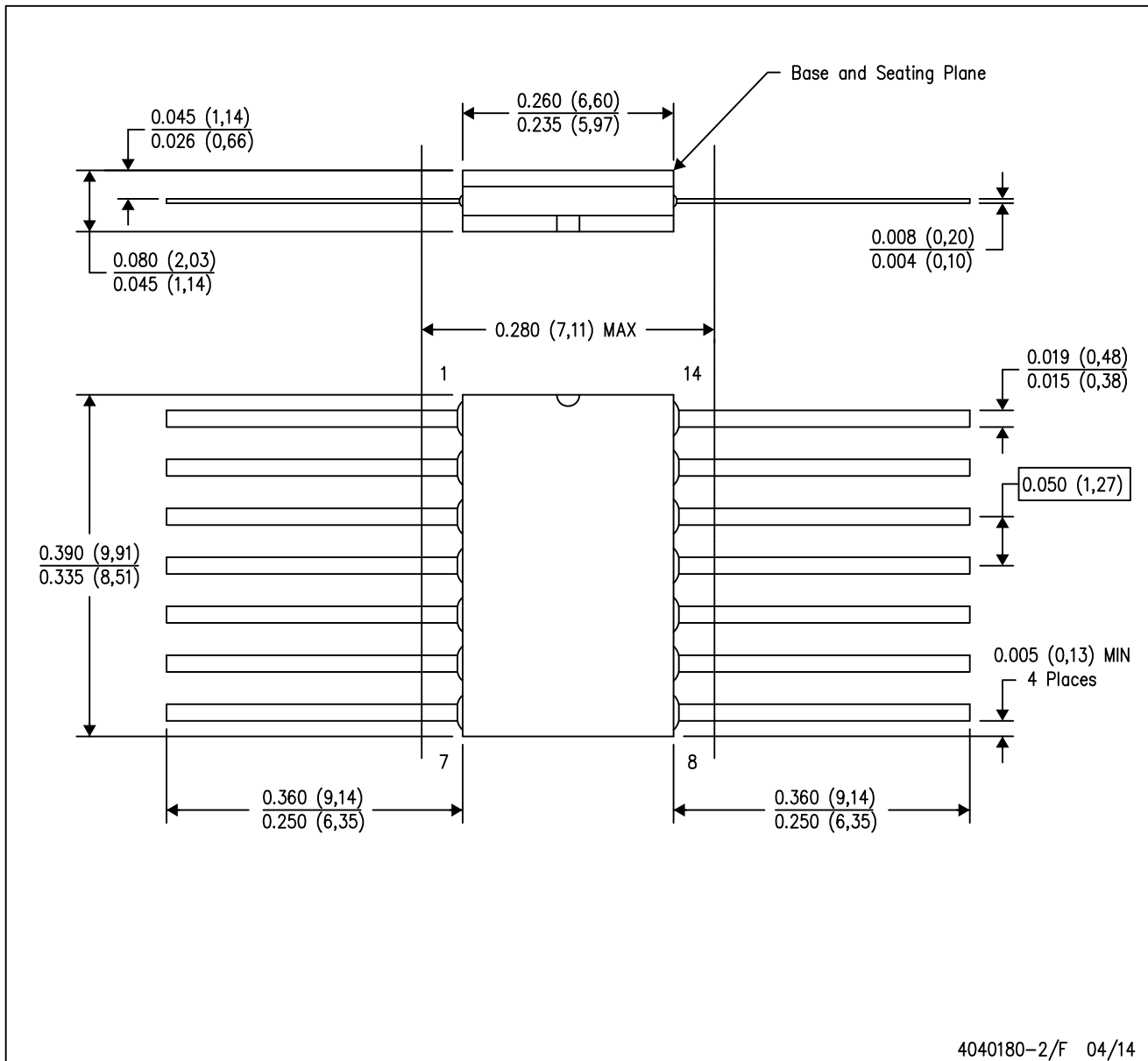


4040179/B 03/95

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

W (R-GDFP-F14)

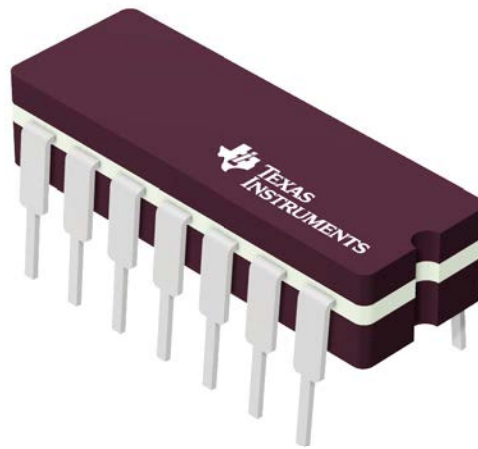
CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

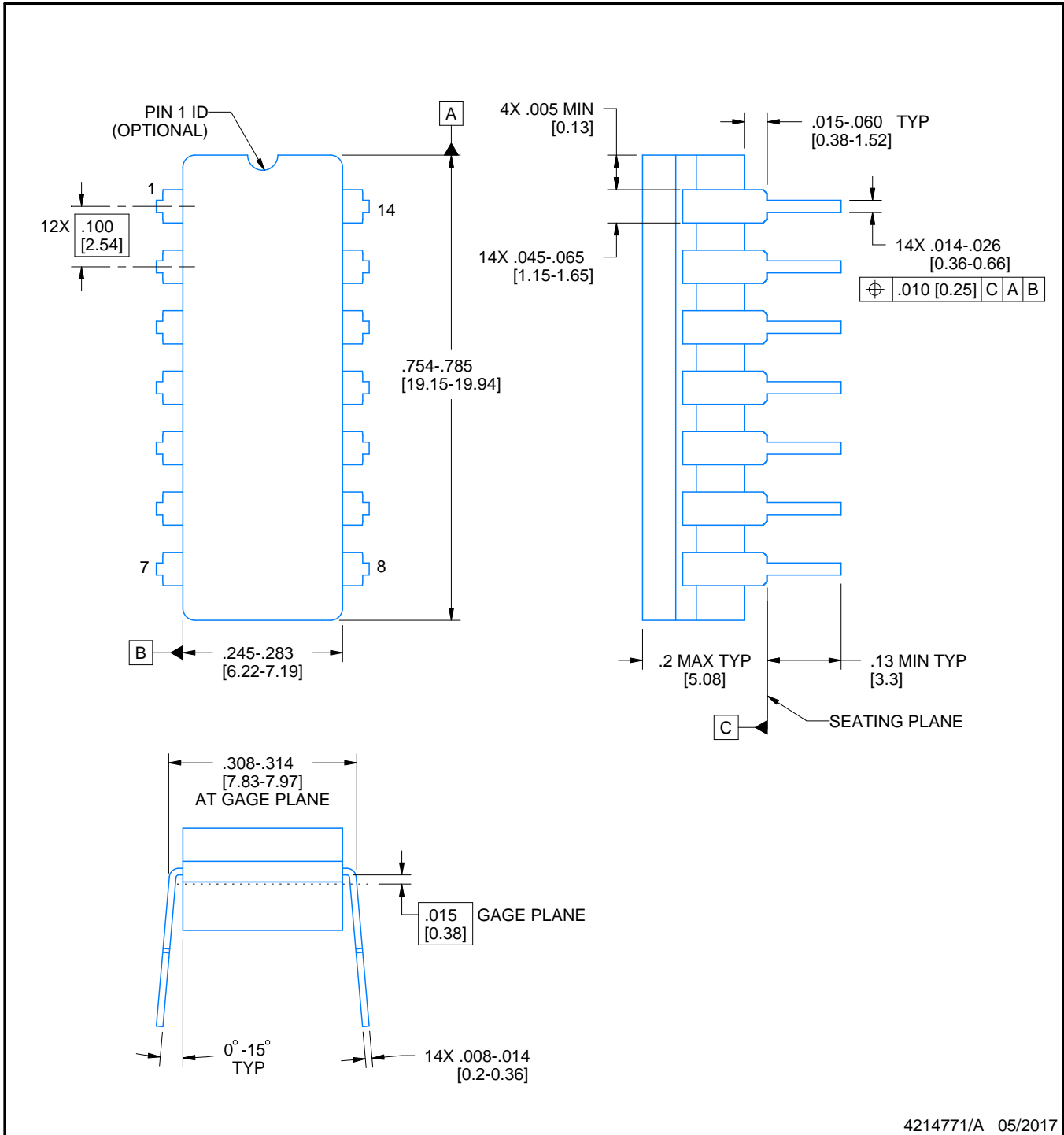
J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

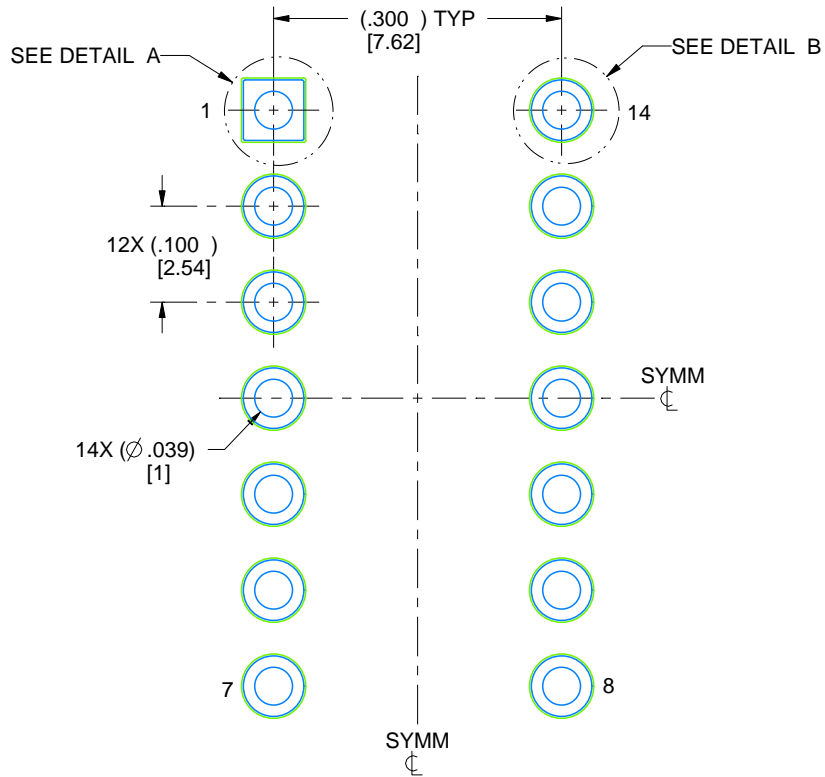
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

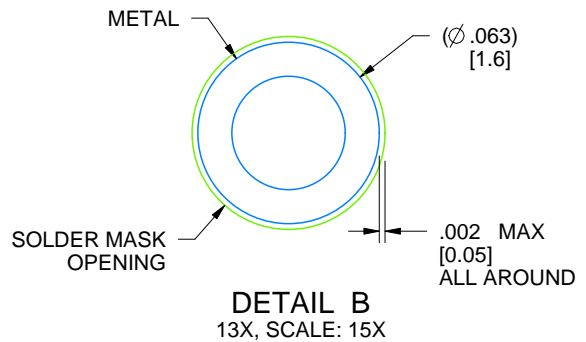
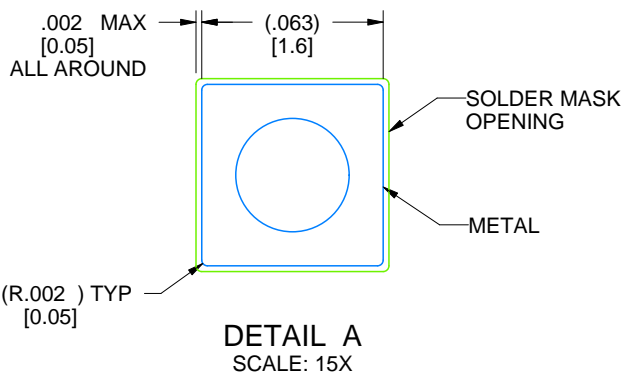
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X

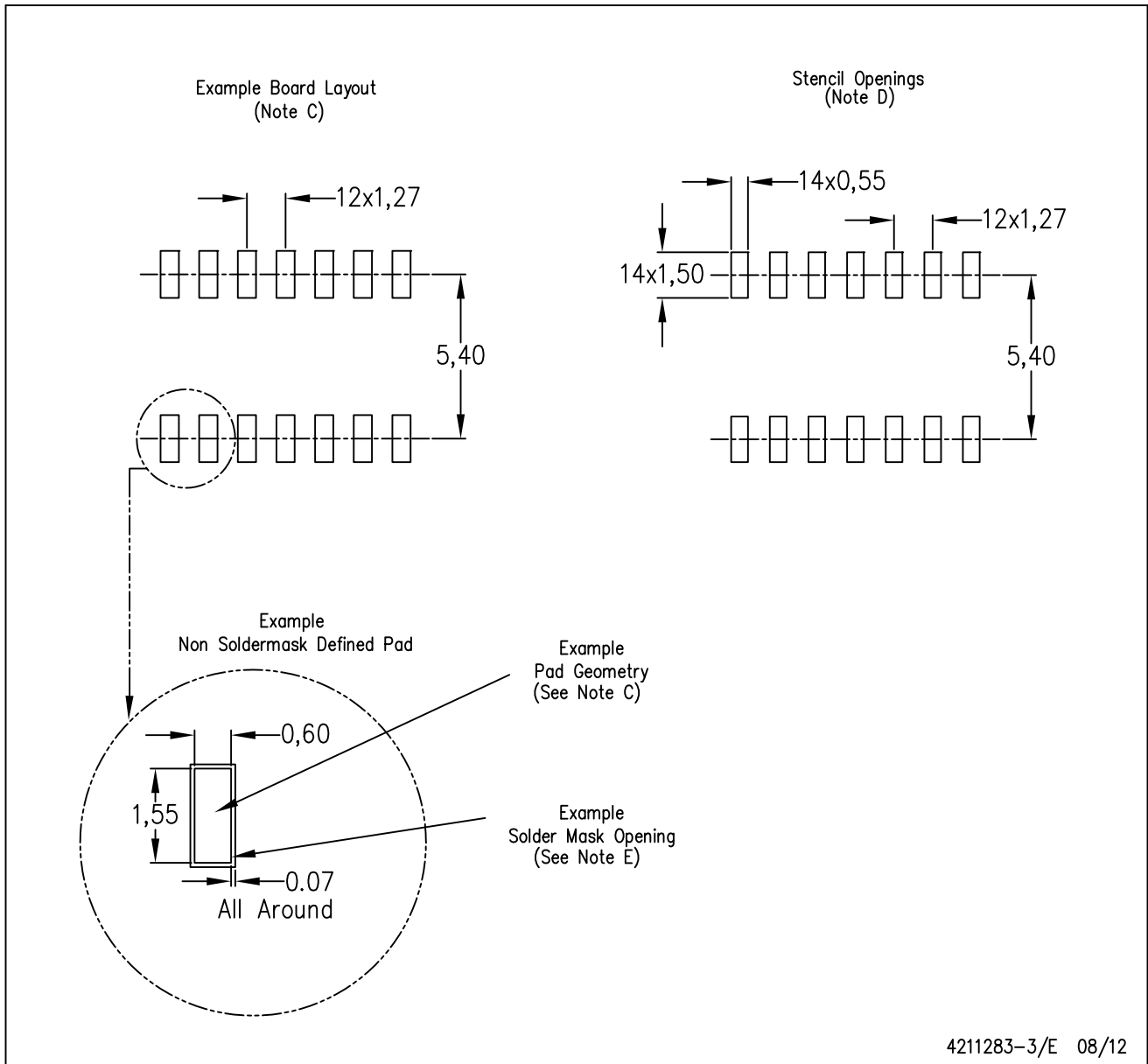


4214771/A 05/2017



D (R-PDSO-G14)

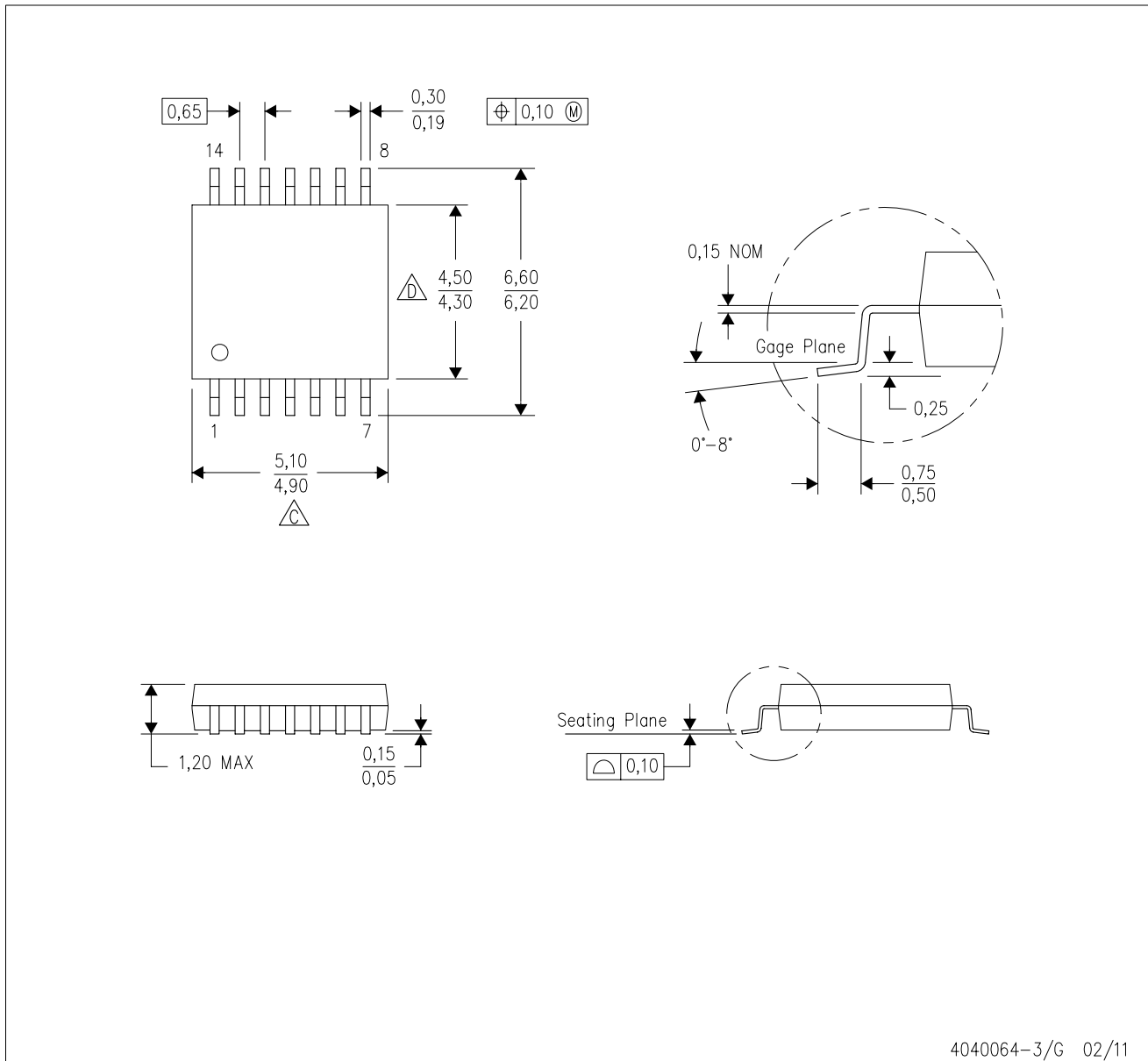
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

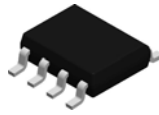
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153



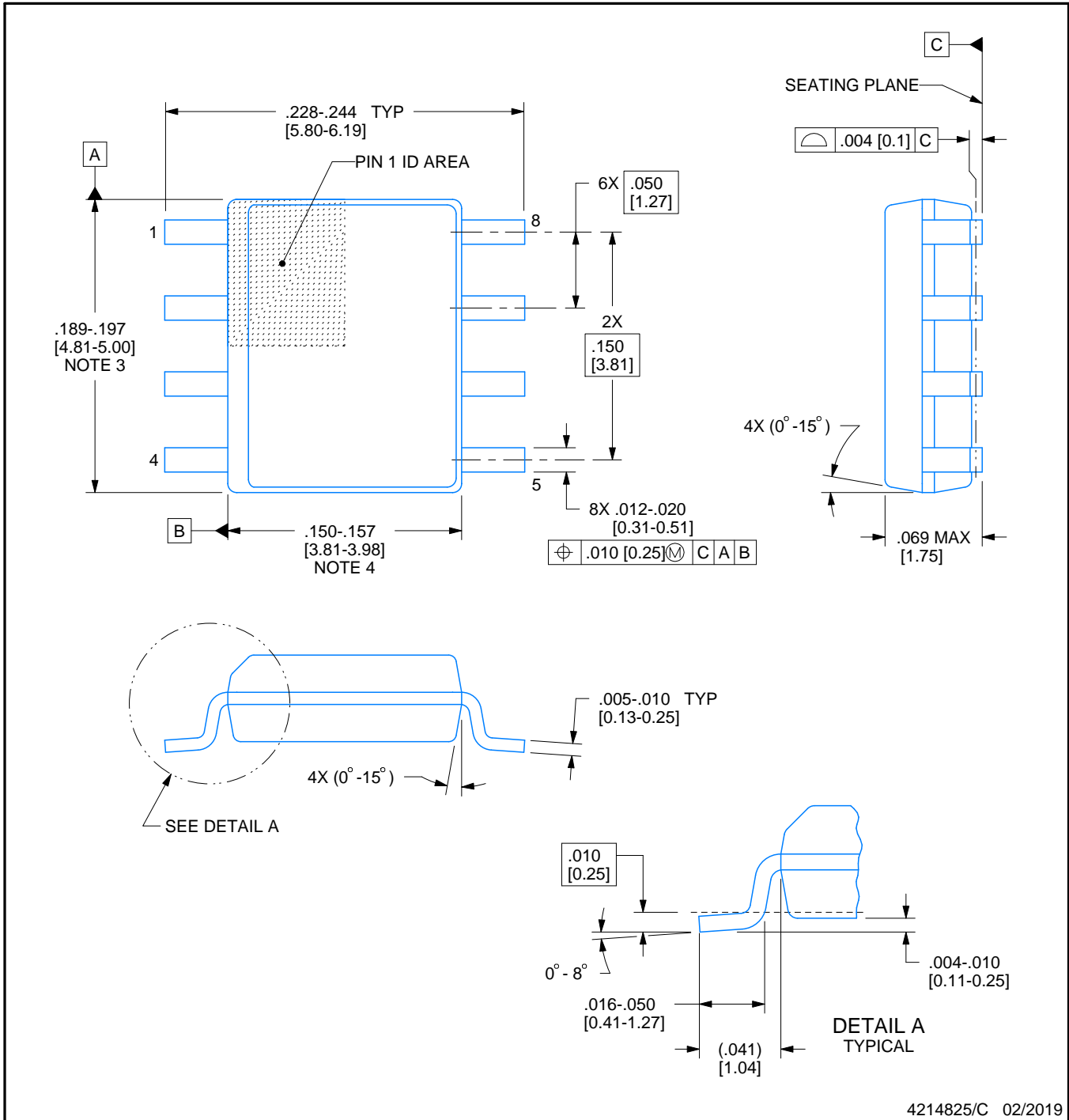


D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

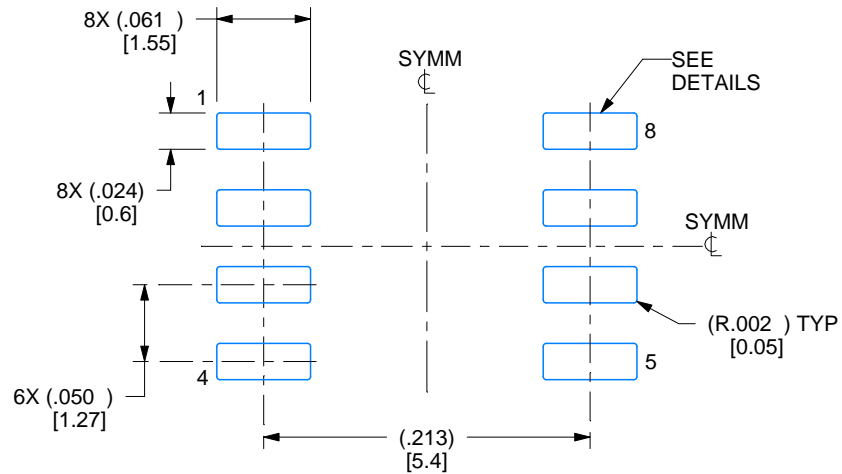
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

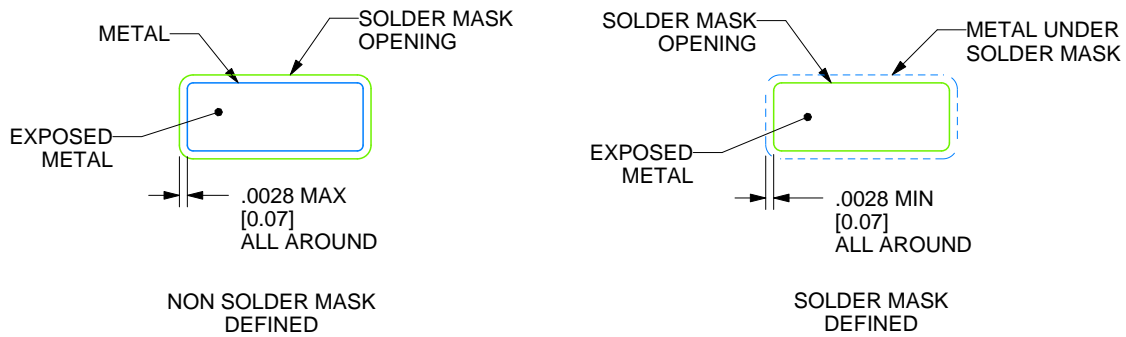
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

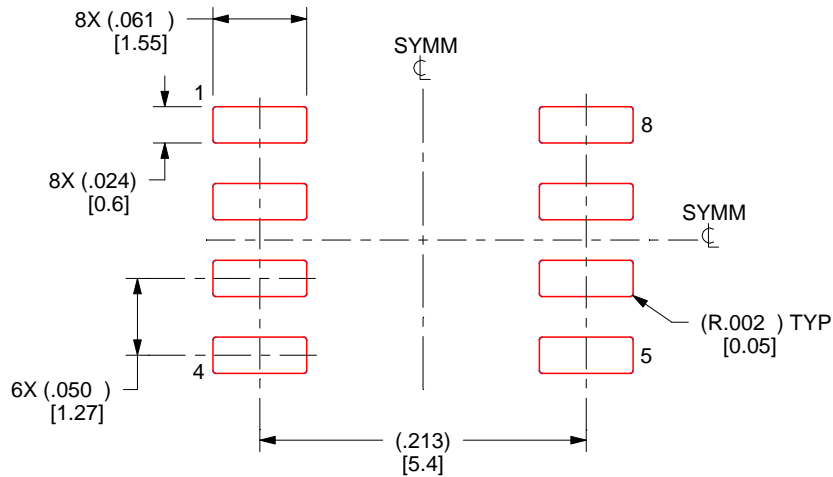
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

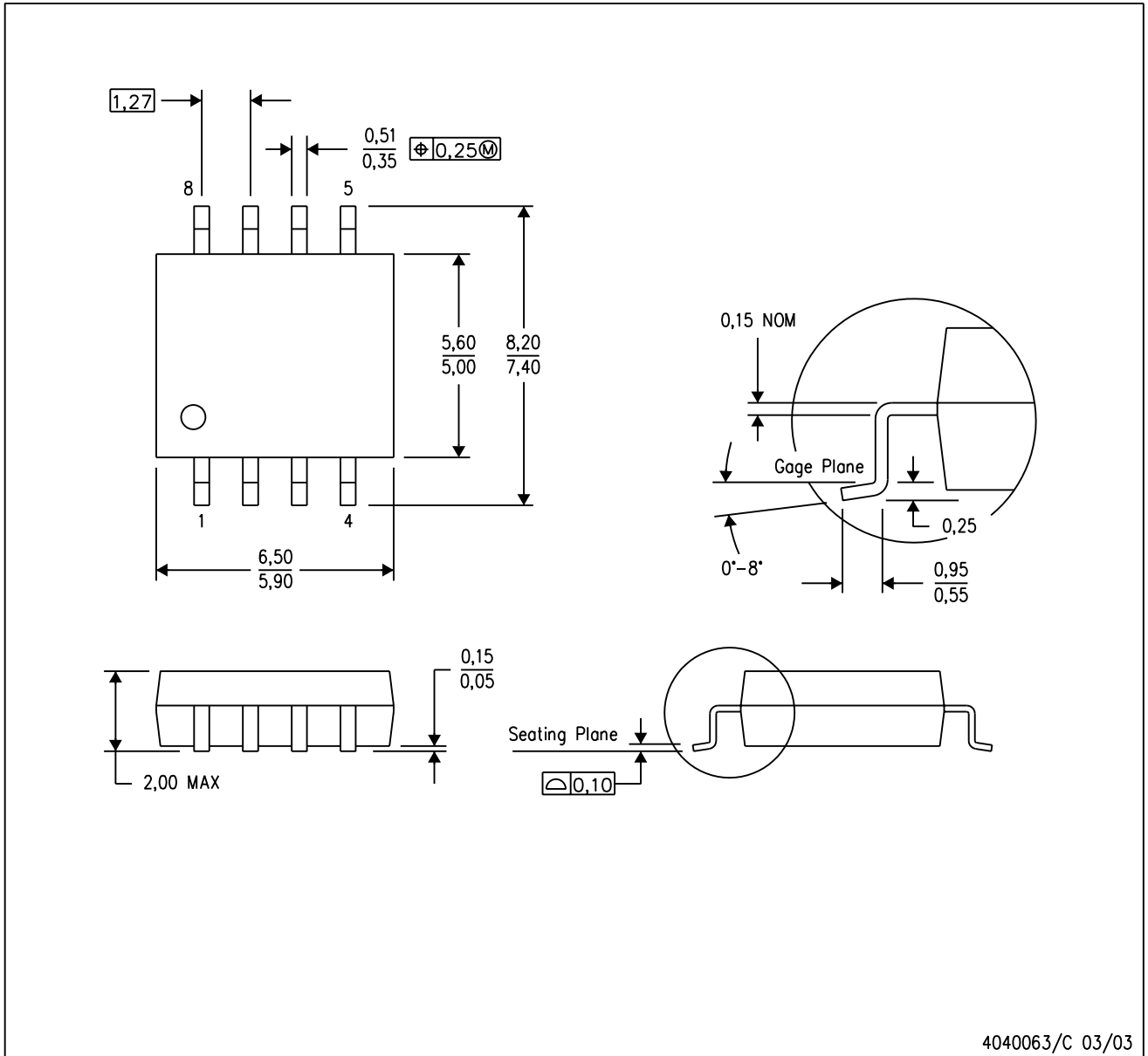
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

PS (R-PDSO-G8)

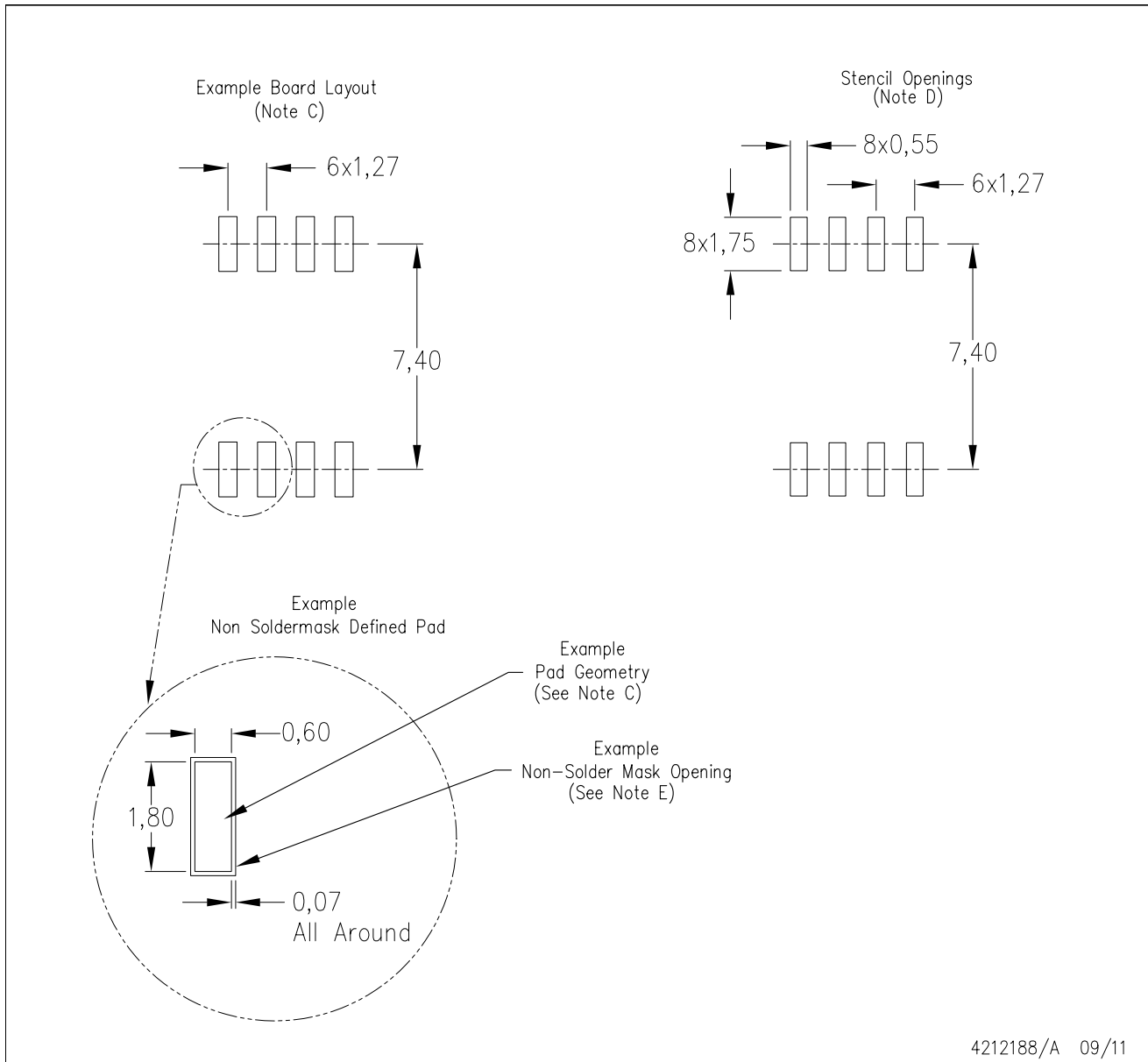
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

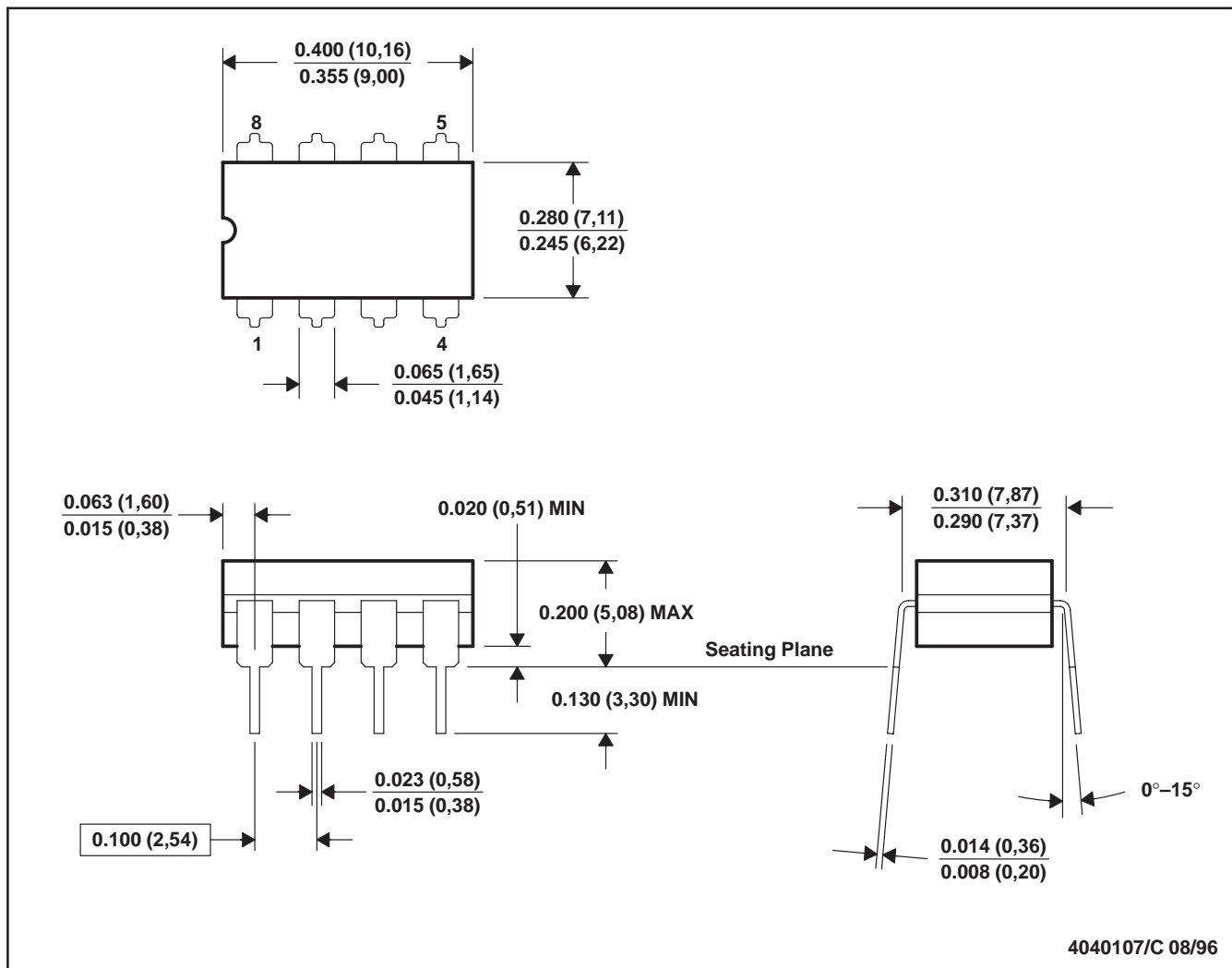
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8)

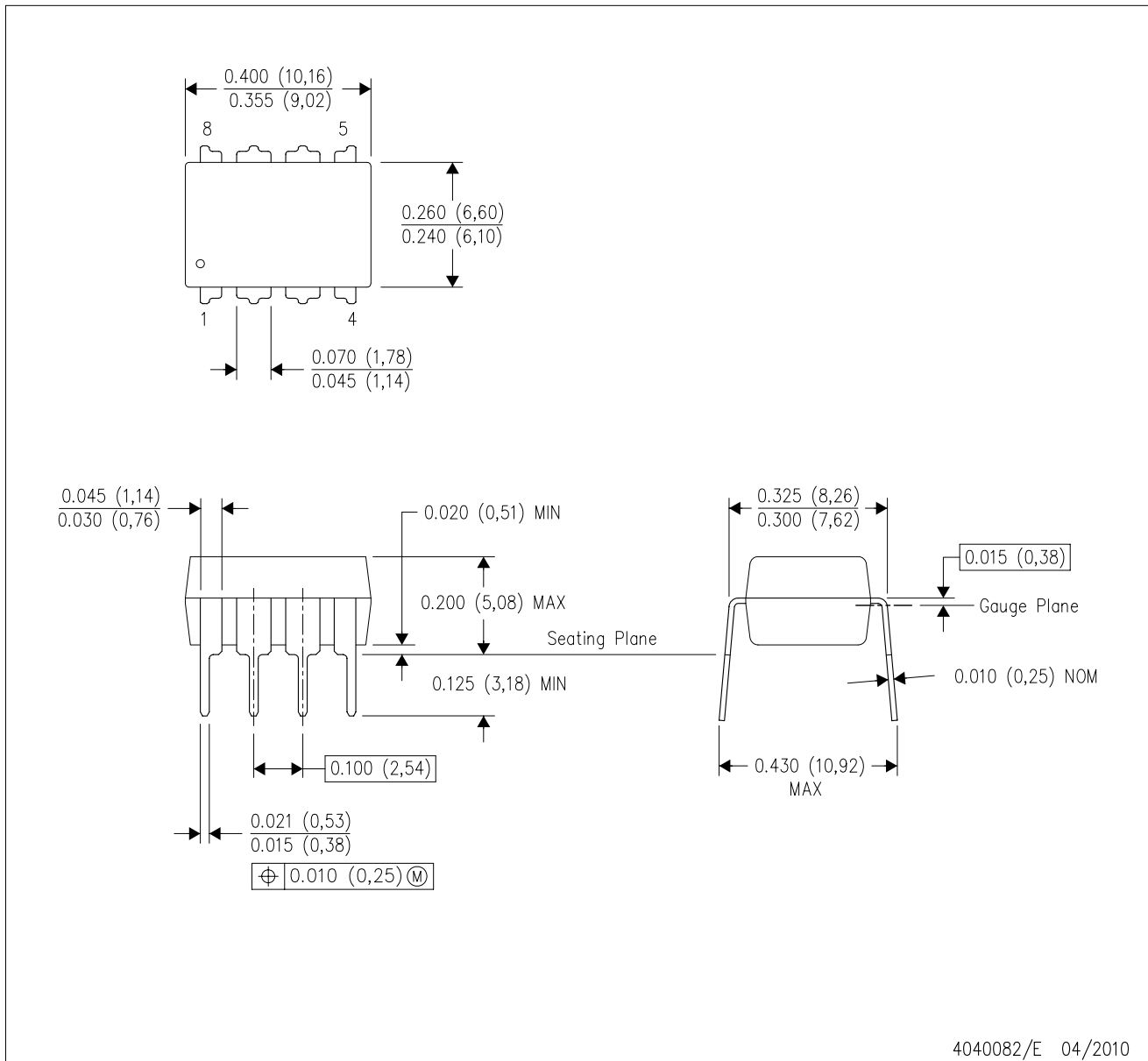
CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

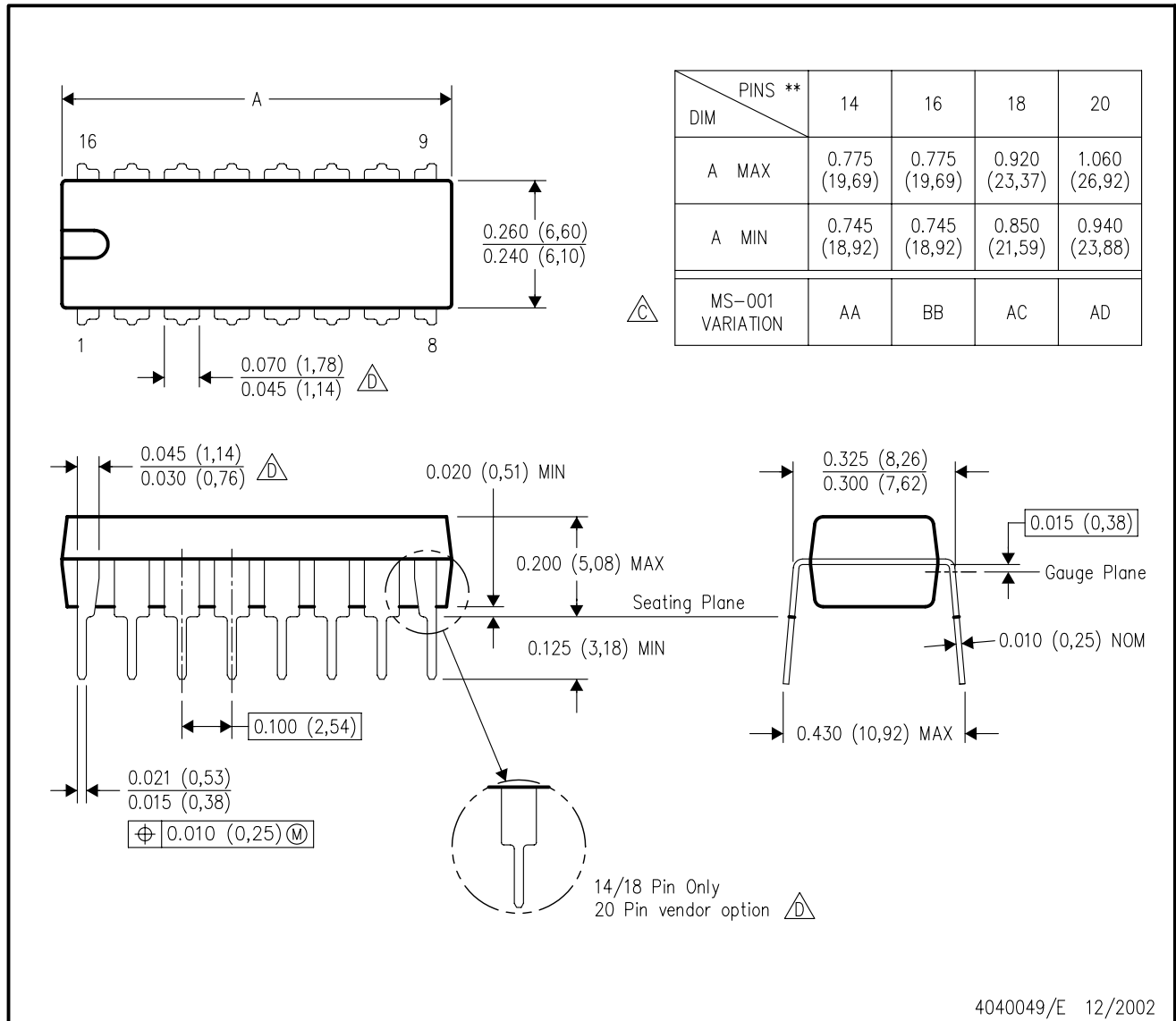


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

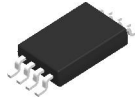


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002



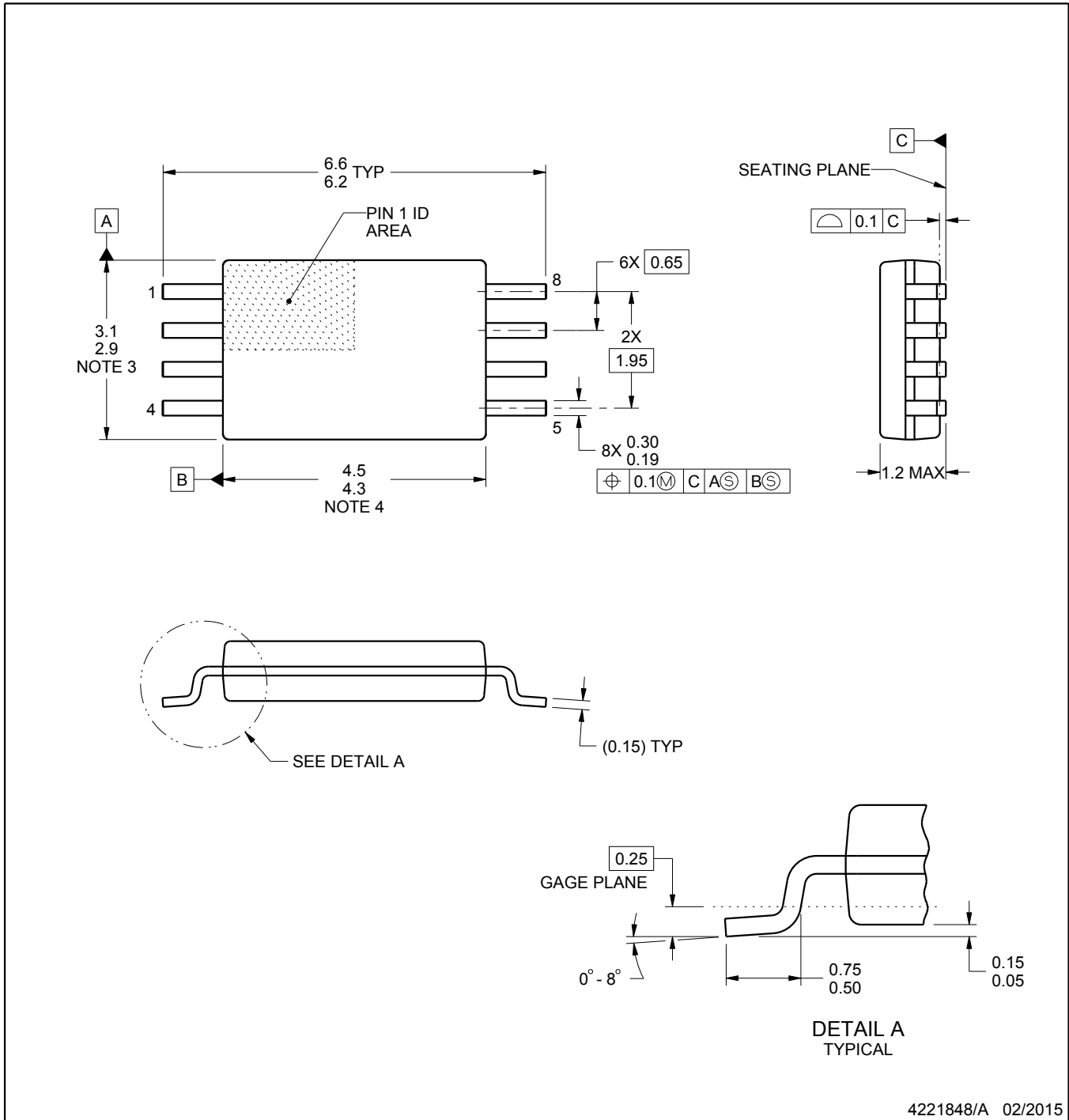
PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

### NOTES:

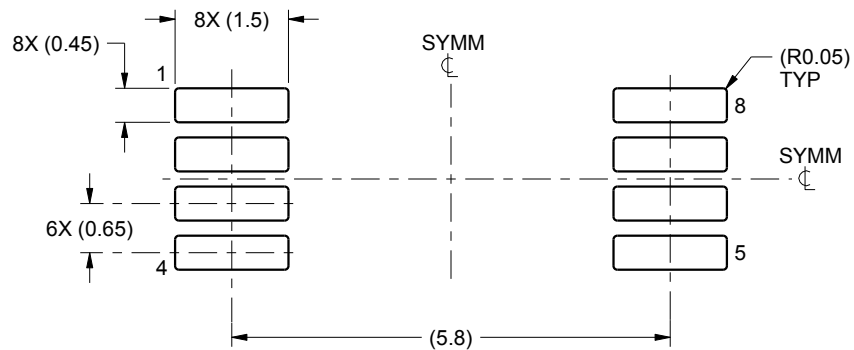
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

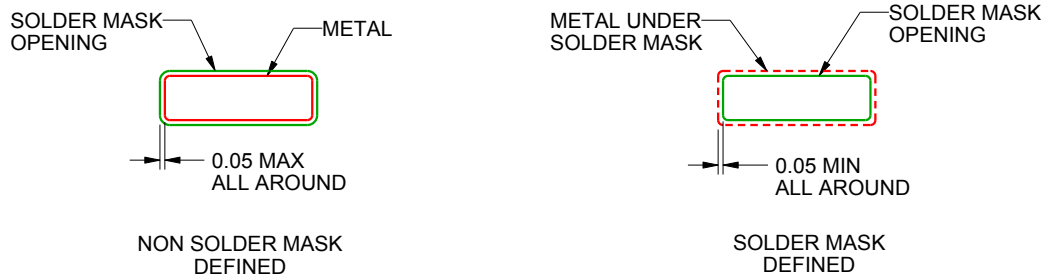
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

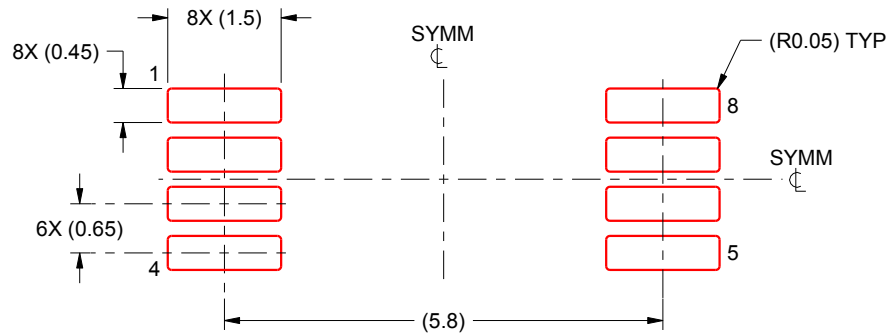
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

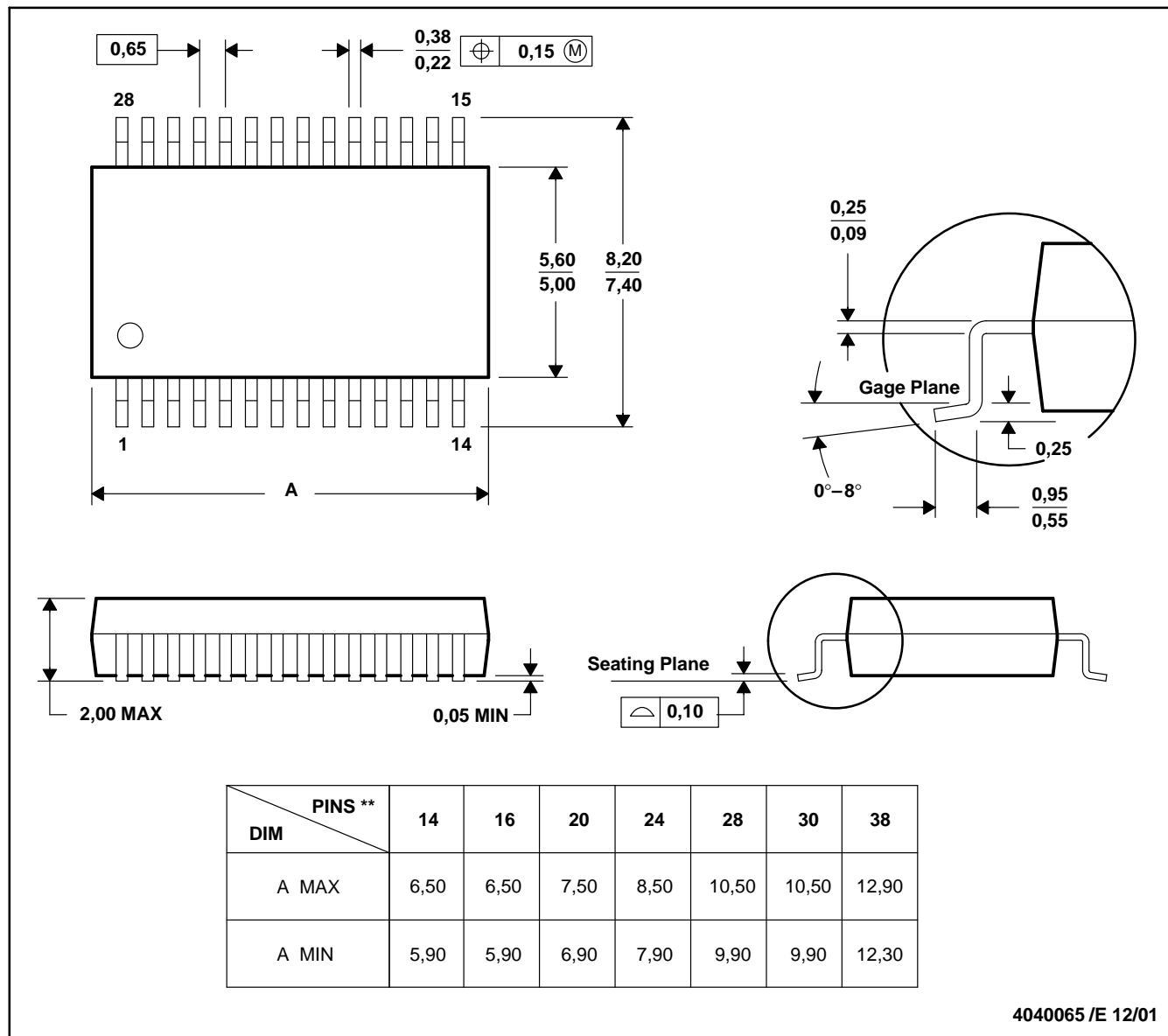
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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