

General Description

- Trench Power AlphaMOS (αMOS LV) technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

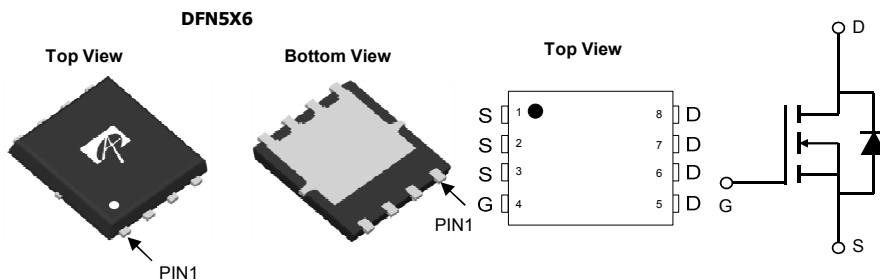
Applications

- DC/DC Converters in Computing
- Isolated DC/DC Converters in Telecom and Industrial
- See Note I

Product Summary

V_{DS}	30V
I_D (at $V_{GS}=10V$)	24A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 6.8mΩ
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 10.5mΩ

100% UIS Tested
 100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON6380	DFN 5x6	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ\text{C}$	24
		$T_C=100^\circ\text{C}$	24
Pulsed Drain Current ^C	I_{DM}	88	A
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	22
		$T_A=70^\circ\text{C}$	17.5
Avalanche Current ^C	I_{AS}	60	A
Avalanche energy $L=0.001\text{mH}$ ^C	E_{AS}	2	mJ
V_{DS} Spike	V_{SPIKE}	36	V
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	26
		$T_C=100^\circ\text{C}$	10.5
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	5
		$T_A=70^\circ\text{C}$	3.2
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	20	25	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A D}				
Maximum Junction-to-Case	$R_{\theta JC}$	3.8	4.8	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.4	1.8	2.2	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		5.6	6.8	mΩ
		V _{GS} =4.5V, I _D =20A		8.1	9.8	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		40		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current ^G				24	A
DYNAMIC PARAMETERS						
C _{ISS}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		825		pF
C _{OSS}	Output Capacitance			335		pF
C _{RSS}	Reverse Transfer Capacitance			40		pF
R _g	Gate resistance	f=1MHz	0.6	1.2	1.8	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		13	25	nC
Q _{g(4.5V)}	Total Gate Charge			6.2	12	nC
Q _{gs}	Gate Source Charge			2.2		nC
Q _{gd}	Gate Drain Charge			2.6		nC
Q _{gs}	Gate Source Charge	V _{GS} =4.5V, V _{DS} =15V, I _D =20A		2.2		nC
Q _{gd}	Gate Drain Charge			2.6		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		5		ns
t _r	Turn-On Rise Time			3		ns
t _{D(off)}	Turn-Off DelayTime			20		ns
t _f	Turn-Off Fall Time			3		ns
t _{rr}	Body Diode Reverse Recovery Time		I _F =20A, di/dt=500A/μs		11	
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=500A/μs		17		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

I. For application requiring slow >1ms turn-on/turn-off, please consult AOS FAE for proper product selection.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

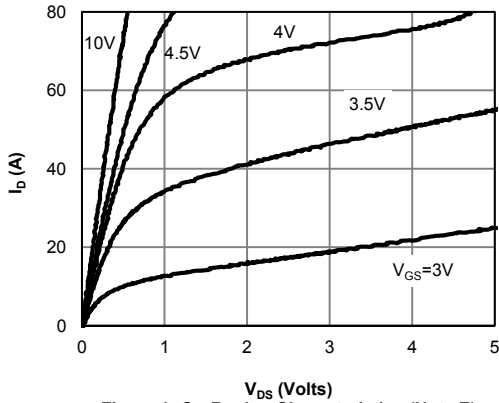


Figure 1: On-Region Characteristics (Note E)

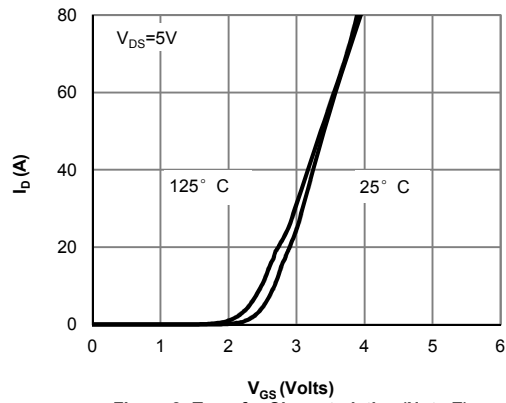


Figure 2: Transfer Characteristics (Note E)

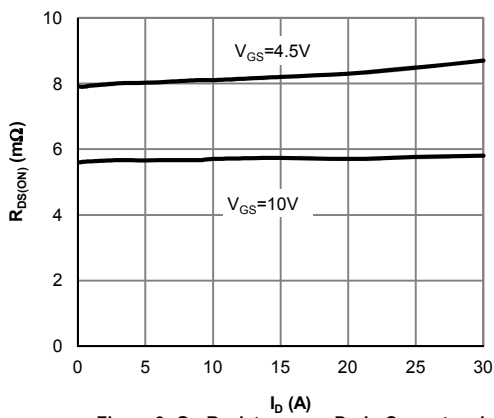


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

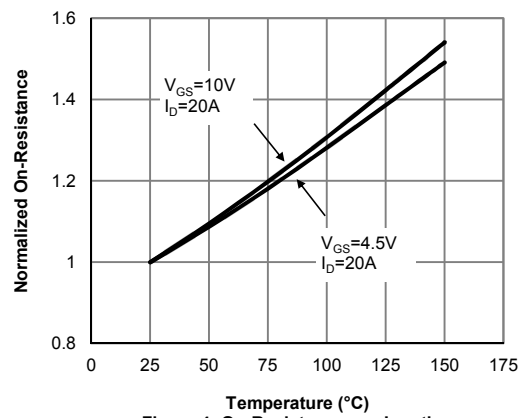


Figure 4: On-Resistance vs. Junction Temperature (Note E)

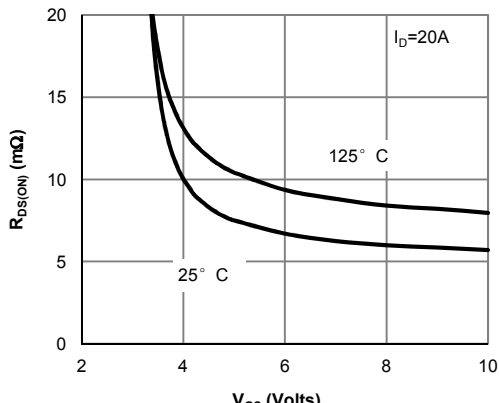


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

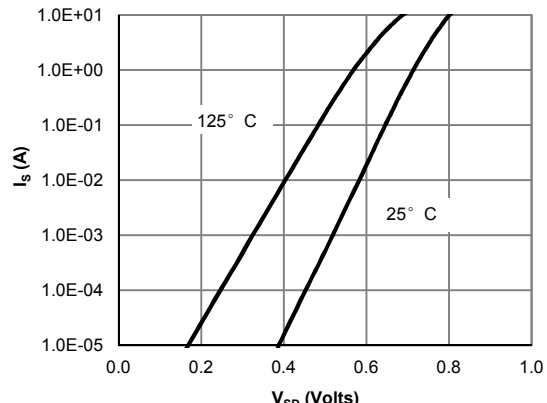


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

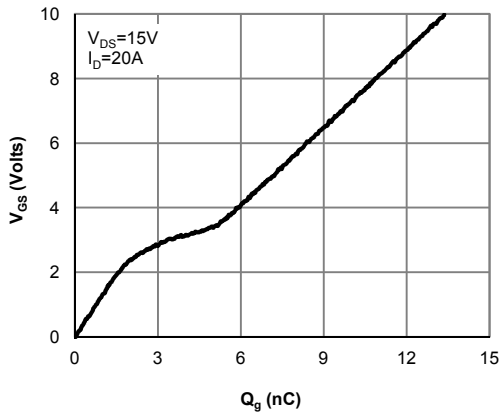


Figure 7: Gate-Charge Characteristics

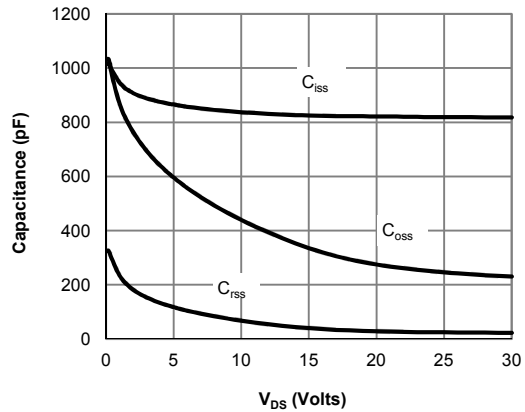


Figure 8: Capacitance Characteristics

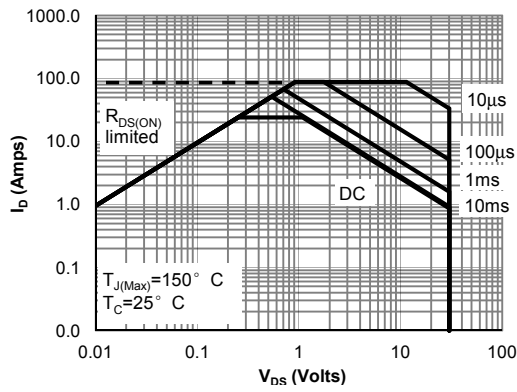


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

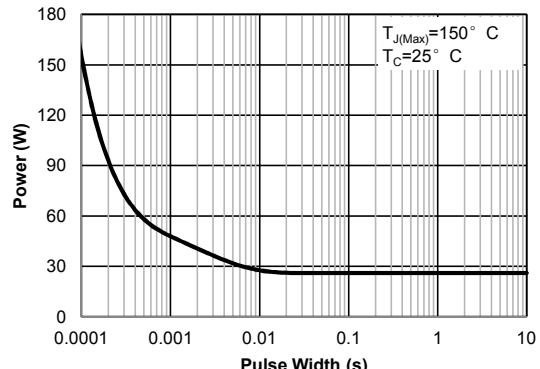


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

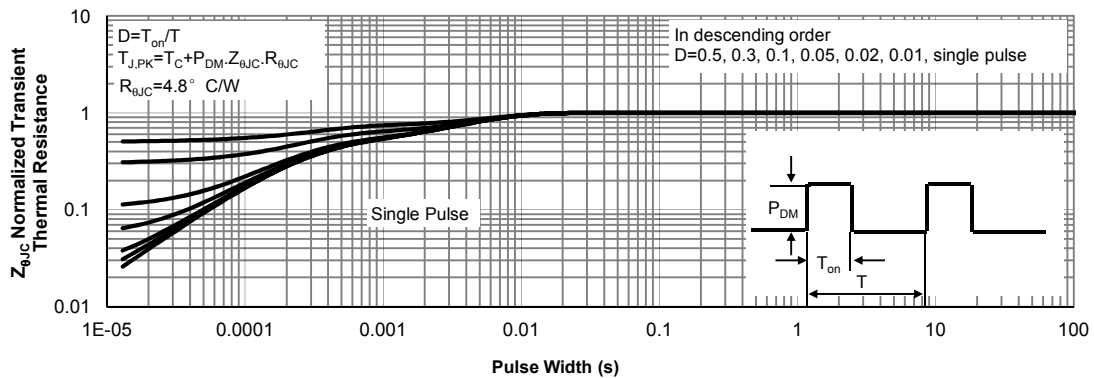


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

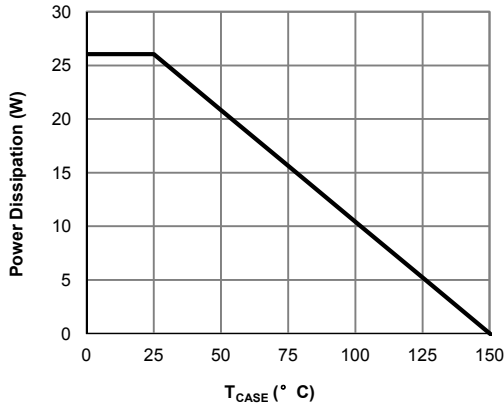


Figure 12: Power De-rating (Note F)

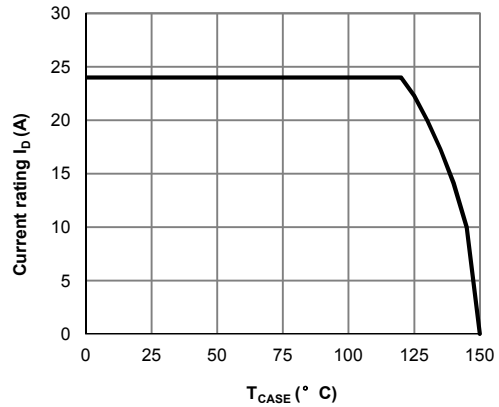


Figure 13: Current De-rating (Note F)

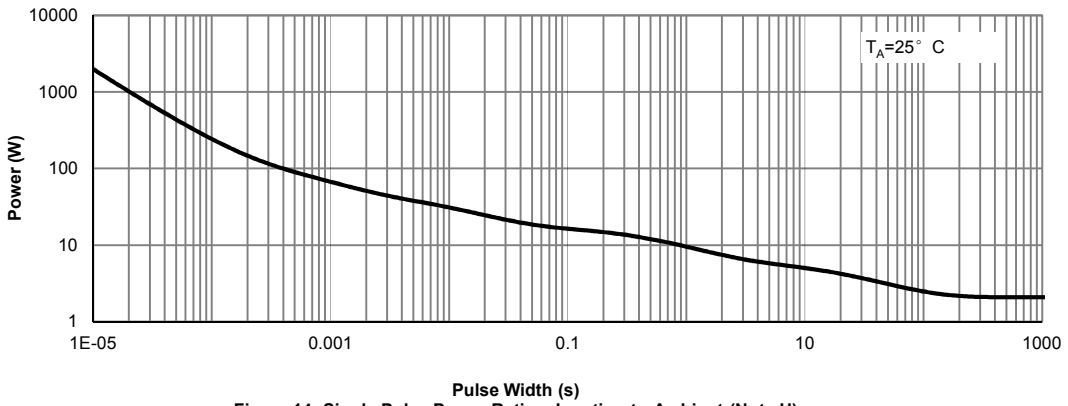


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

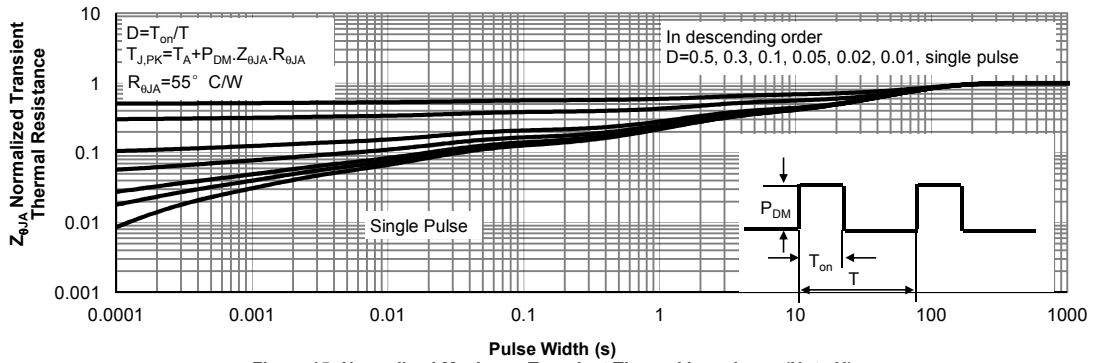


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

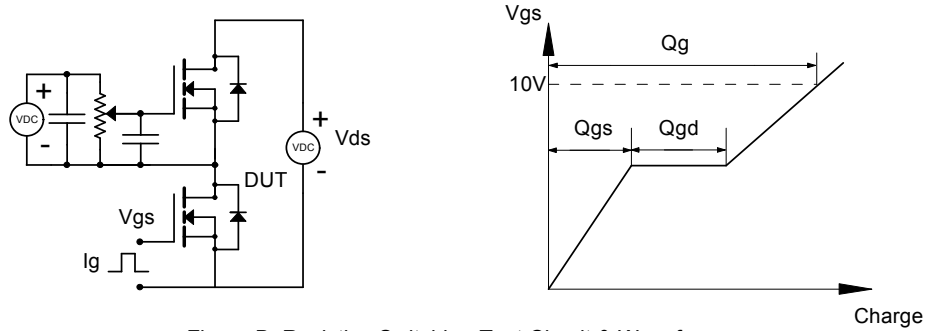


Figure B: Resistive Switching Test Circuit & Waveforms

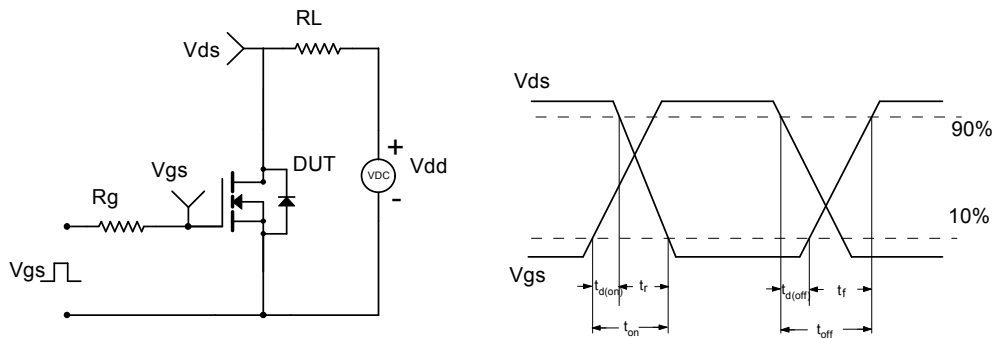


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

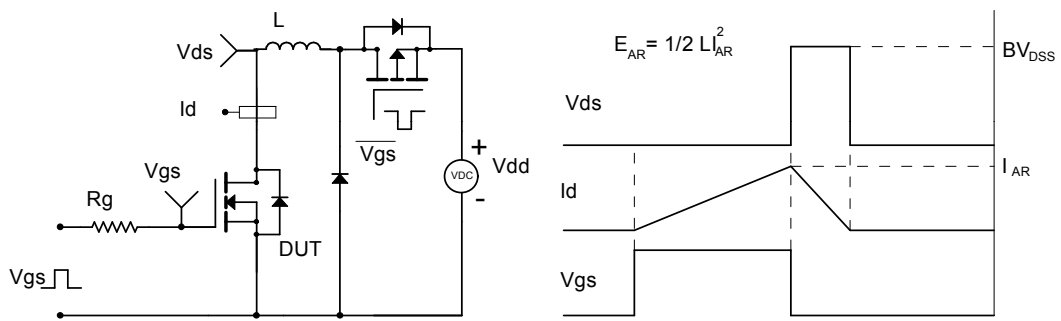


Figure D: Diode Recovery Test Circuit & Waveforms

