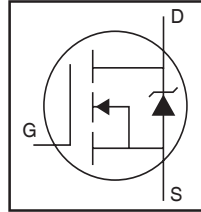


HEXFET® Power MOSFET

## Applications

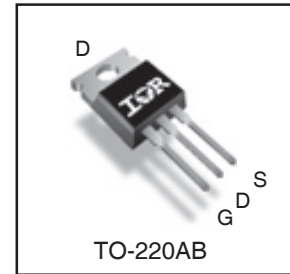
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



$V_{DSS}$		<b>150V</b>
$R_{DS(on)}$	typ.	<b>9.3mΩ</b>
	max.	<b>11mΩ</b>
$I_D$ (Silicon Limited)		<b>104A</b>

## Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead Free
- RoHS Compliant, Halogen-Free



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB4115PbF	TO-220	Tube	50	IRFB4115PbF

## Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	104	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	74	
$I_{DM}$	Pulsed Drain Current ①	420	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	380	W
	Linear Derating Factor	2.5	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ③	18	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

## Avalanche Characteristics

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	830	mJ
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## Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	0.40	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑦⑧	—	62	

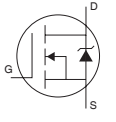
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	150	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/°C	Reference to 25°C, I <sub>D</sub> = 3.5mA <sup>①</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	9.3	11	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 62A <sup>④</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0	—	5.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 150V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 150V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
R <sub>G</sub>	Internal Gate Resistance	—	2.3	—	Ω	

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

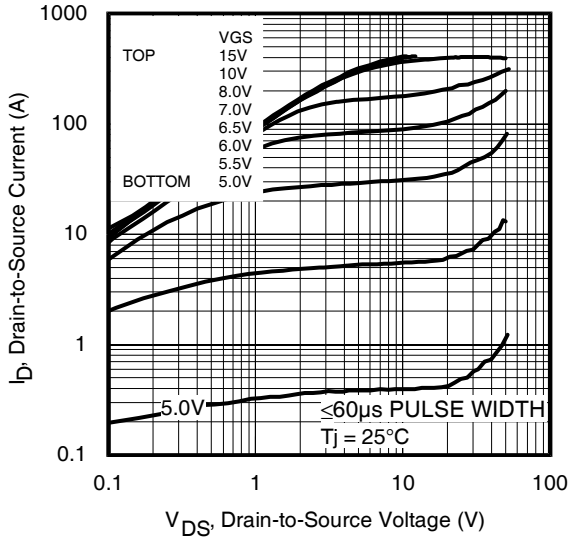
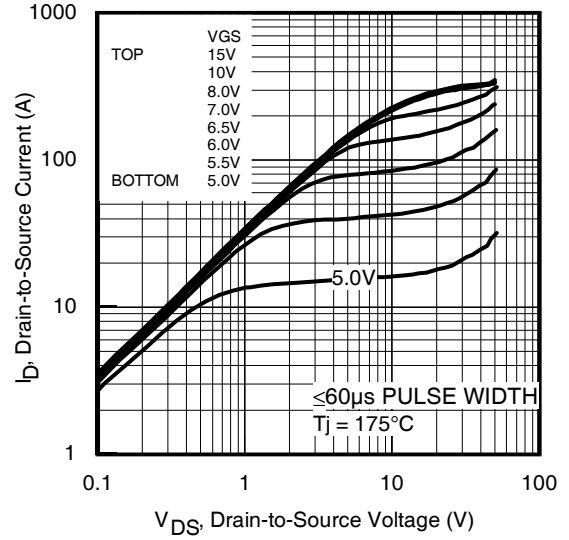
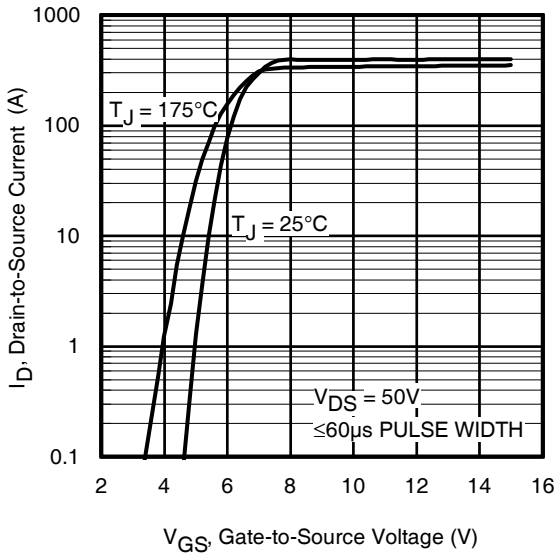
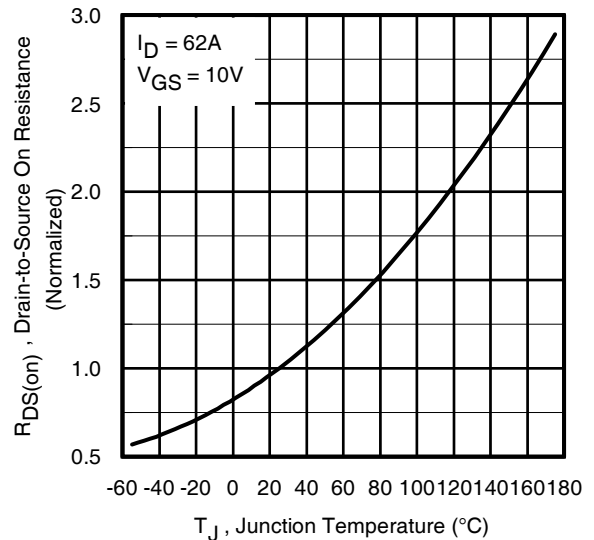
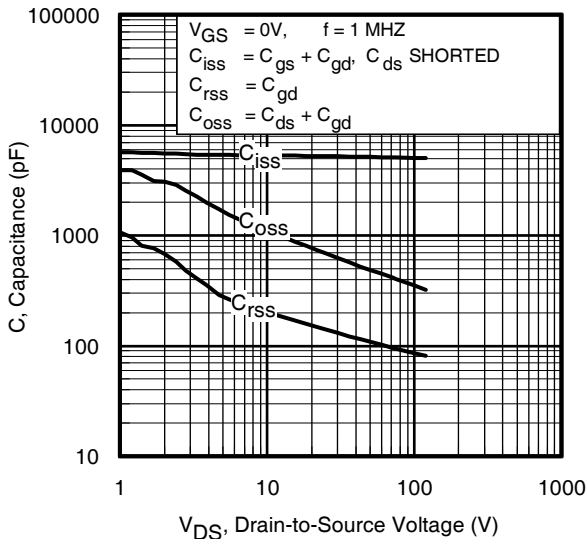
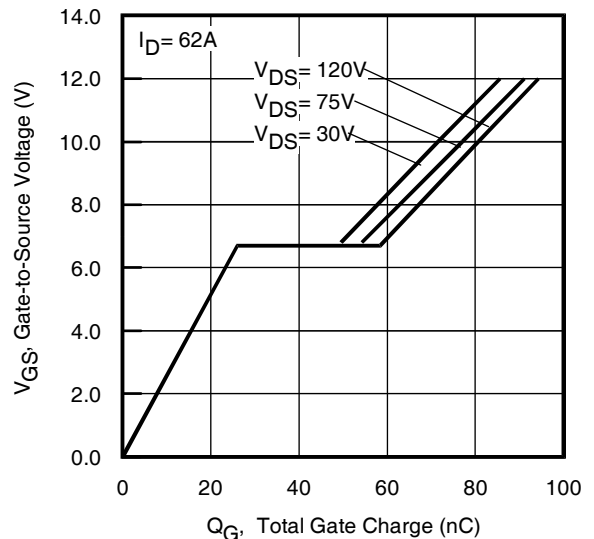
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	97	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 62A
Q <sub>g</sub>	Total Gate Charge	—	77	120	nC	I <sub>D</sub> = 62A
Q <sub>gs</sub>	Gate-to-Source Charge	—	28	—		V <sub>DS</sub> = 75V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	26	—		V <sub>GS</sub> = 10V <sup>④</sup>
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	51	—		I <sub>D</sub> = 62A, V <sub>DS</sub> = 0V, V <sub>GS</sub> = 10V
t <sub>d(on)</sub>	Turn-On Delay Time	—	18	—	ns	V <sub>DD</sub> = 98V
t <sub>r</sub>	Rise Time	—	73	—		I <sub>D</sub> = 62A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	41	—		R <sub>G</sub> = 2.2Ω
t <sub>f</sub>	Fall Time	—	39	—		V <sub>GS</sub> = 10V <sup>④</sup>
C <sub>iss</sub>	Input Capacitance	—	5270	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	490	—		V <sub>DS</sub> = 50V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	105	—		f = 1.0 MHz, See Fig. 5
C <sub>oss</sub> eff. (ER)	Effective Output Capacitance (Energy Related)	—	460	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 120V <sup>⑥</sup> , See Fig. 11
C <sub>oss</sub> eff. (TR)	Effective Output Capacitance (Time Related)	—	530	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 120V <sup>⑤</sup>

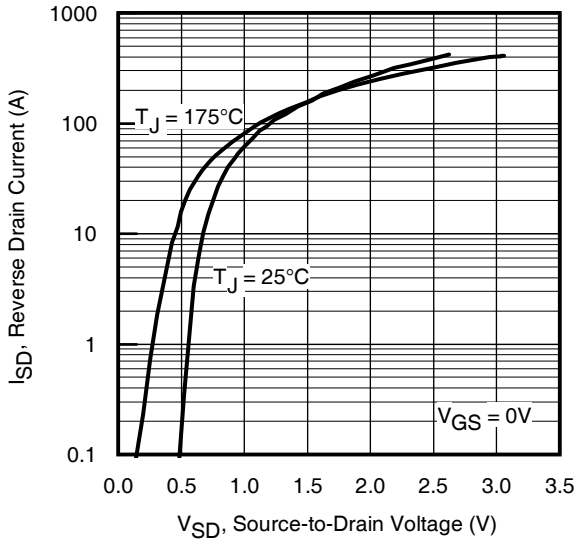
**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	104	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>②</sup>	—	—	420	A	
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 62A, V <sub>GS</sub> = 0V <sup>④</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	86	—	ns	T <sub>J</sub> = 25°C V <sub>R</sub> = 130V,
		—	110	—		T <sub>J</sub> = 125°C I <sub>F</sub> = 62A
Q <sub>rr</sub>	Reverse Recovery Charge	—	300	—	nC	T <sub>J</sub> = 25°C di/dt = 100A/μs <sup>④</sup>
		—	450	—		T <sub>J</sub> = 125°C
I <sub>RRM</sub>	Reverse Recovery Current	—	6.5	—	A	T <sub>J</sub> = 25°C
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

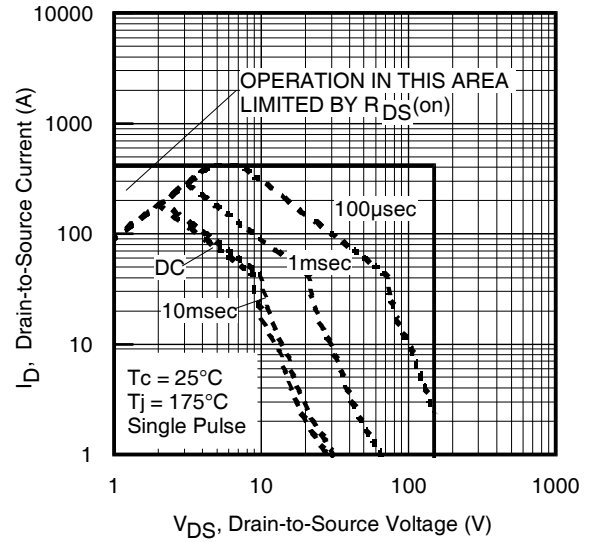
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Recommended max EAS limit, starting T<sub>J</sub> = 25°C, L = 0.17mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 100A, V<sub>GS</sub> = 15V.
- ③ I<sub>SD</sub> ≤ 62A, di/dt ≤ 1040A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C<sub>oss</sub> eff. (TR) is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑥ C<sub>oss</sub> eff. (ER) is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.

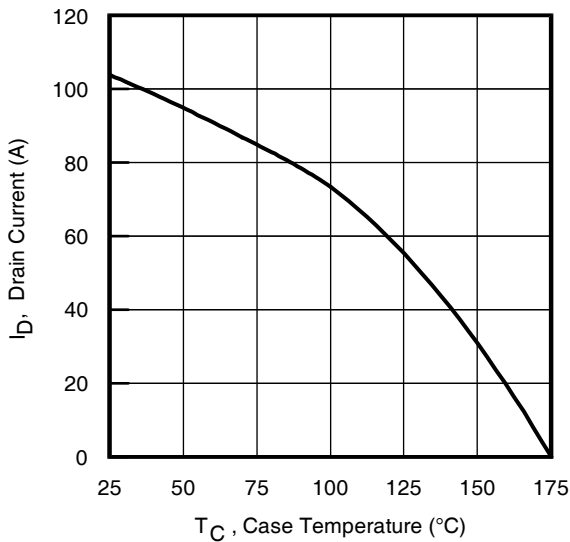

**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**



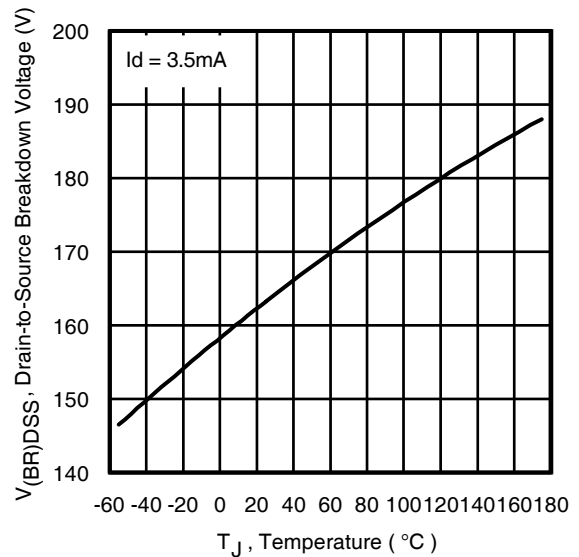
**Fig 7.** Typical Source-Drain Diode Forward Voltage



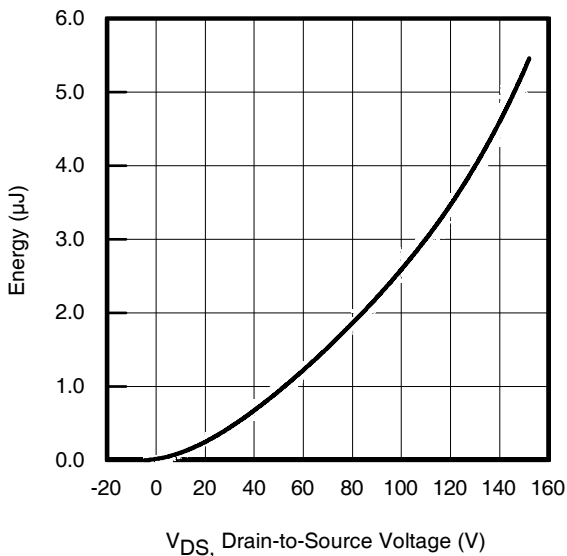
**Fig 8.** Maximum Safe Operating Area



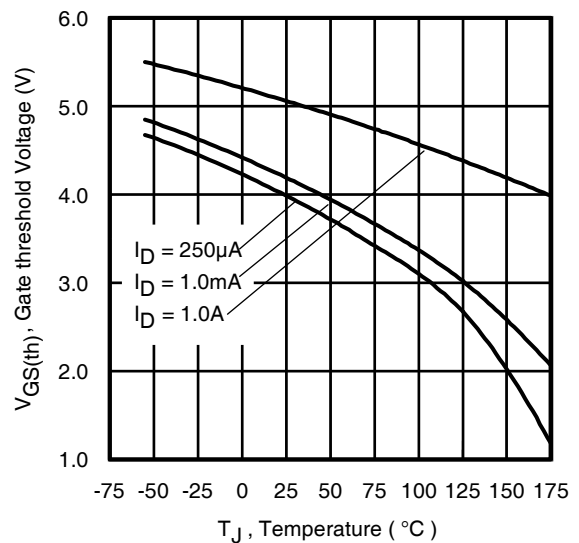
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Drain-to-Source Breakdown Voltage



**Fig 11.** Typical  $C_{OSS}$  Stored Energy



**Fig 12.** Threshold Voltage vs. Temperature

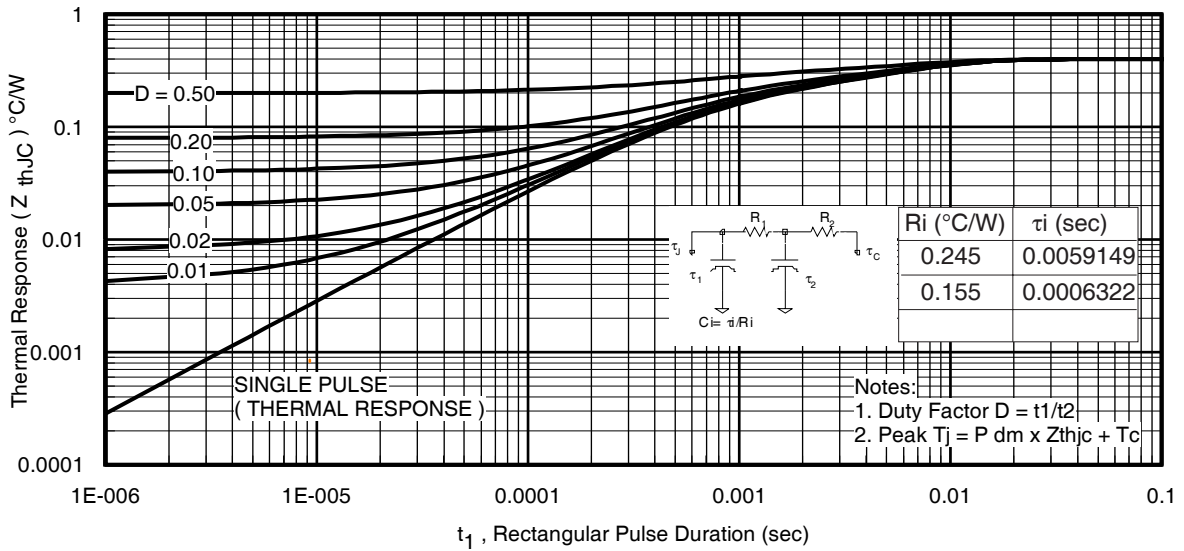


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

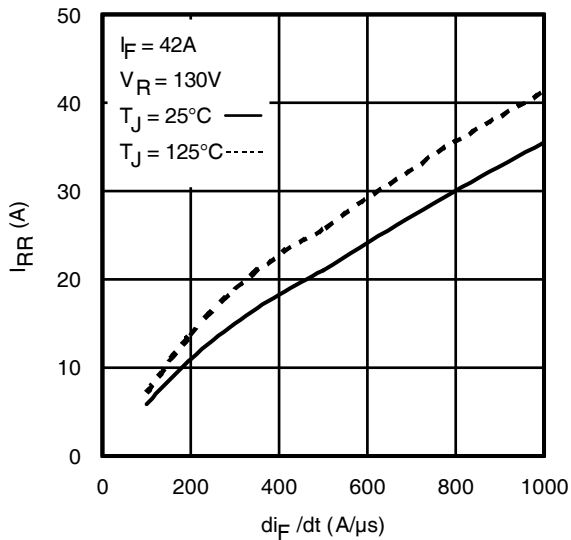


Fig 14. - Typical Recovery Current vs. di<sub>F</sub>/dt

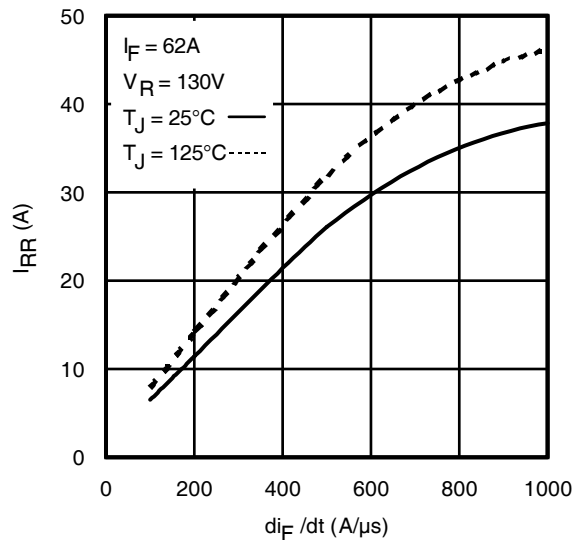


Fig 15. - Typical Recovery Current vs. di<sub>F</sub>/dt

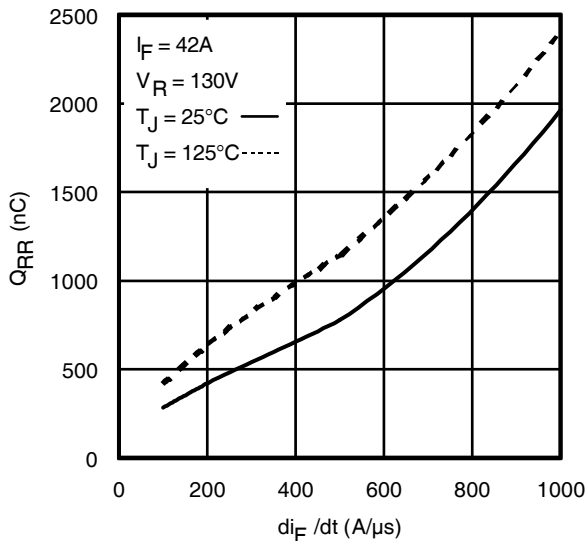


Fig 16. - Typical Stored Charge vs. di<sub>F</sub>/dt

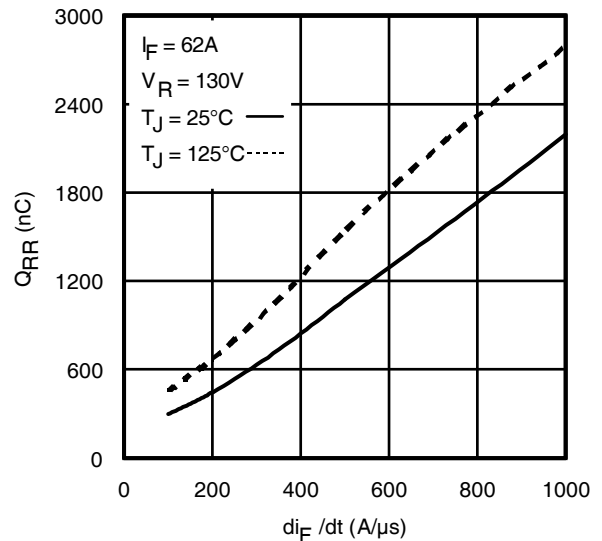
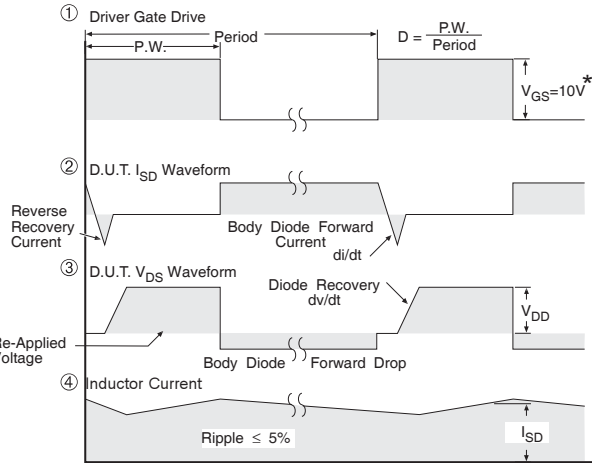
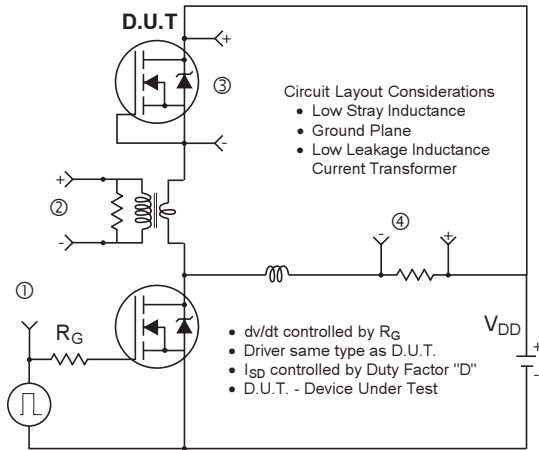
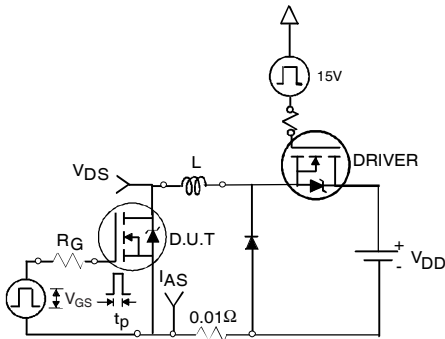


Fig 17. - Typical Stored Charge vs. di<sub>F</sub>/dt

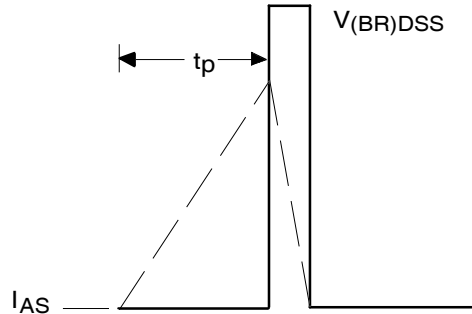


\*  $V_{GS} = 5V$  for Logic Level Devices

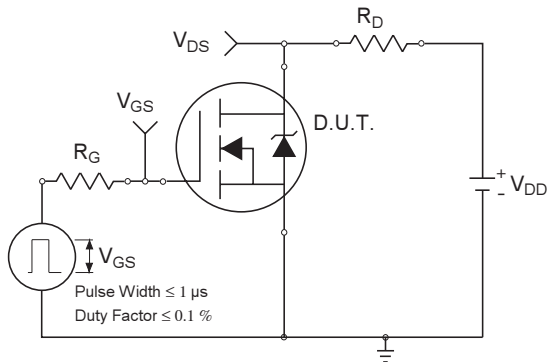
**Fig 18. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



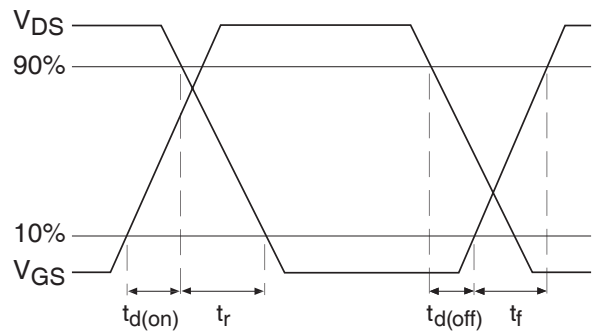
**Fig 19a. Unclamped Inductive Test Circuit**



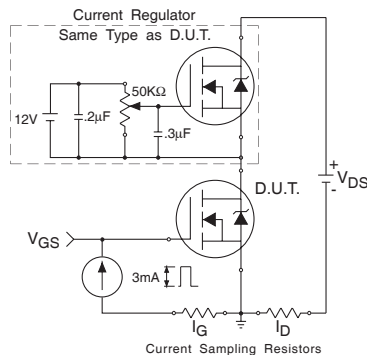
**Fig 19b. Unclamped Inductive Waveforms**



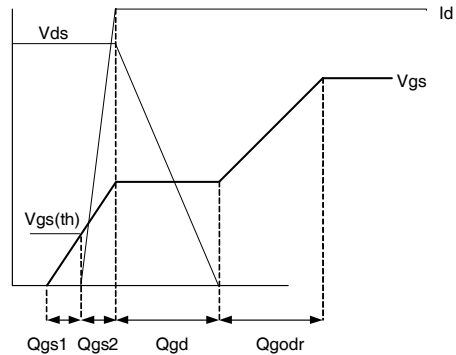
**Fig 20a. Switching Time Test Circuit**



**Fig 20b. Switching Time Waveforms**



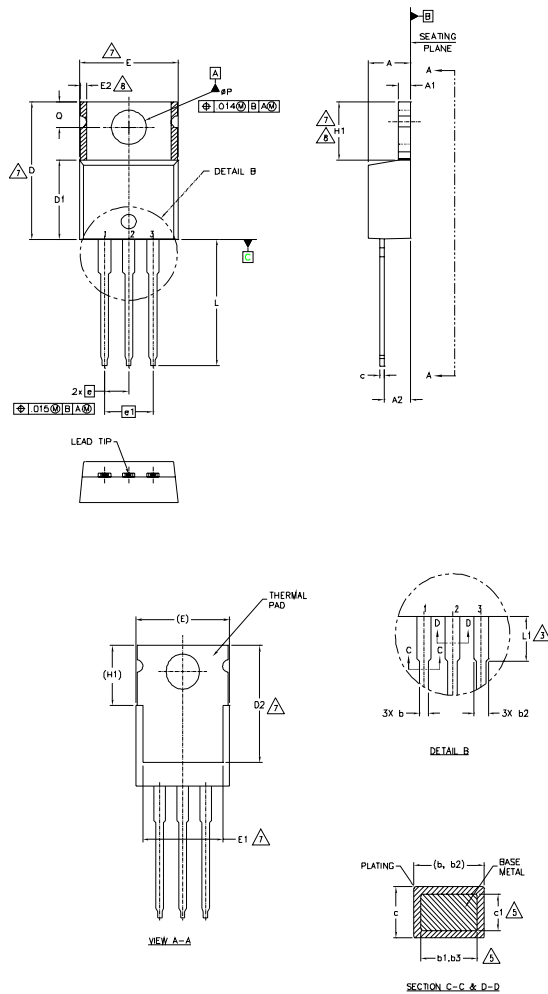
**Fig 21a. Gate Charge Test Circuit**



**Fig 21b. Gate Charge Waveform**

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

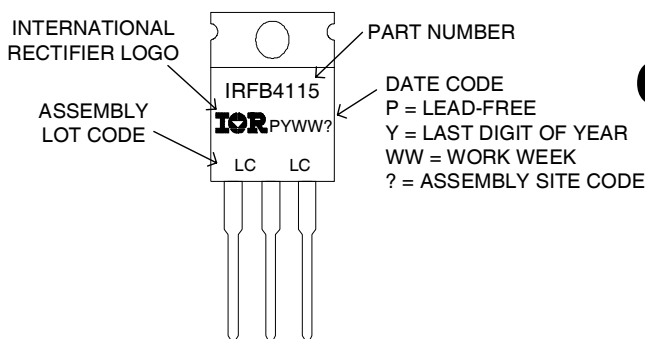


- NOTES:
- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
  - 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
  - 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
  - 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
  - 6.- CONTROLLING DIMENSION : INCHES.
  - 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
  - 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
  - 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

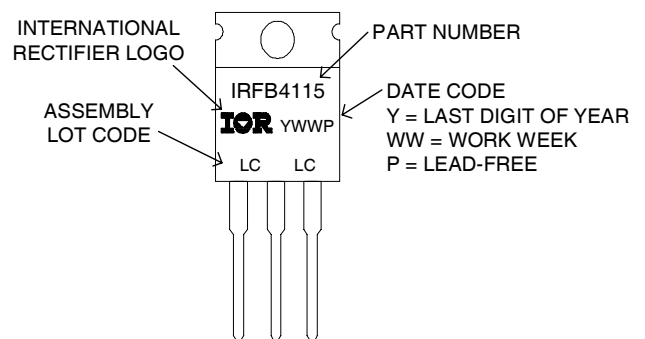
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

- LEAD ASSIGNMENTS
- HEXFET
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE
- IGBTs, CoPACK
- 1.- GATE
  - 2.- COLLECTOR
  - 3.- EMITTER
- DIODES
- 1.- ANODE
  - 2.- CATHODE
  - 3.- ANODE

## TO-220AB Part Marking Information



OR



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

**Qualification information<sup>†</sup>**

Qualification level	Industrial <sup>†</sup>	
	(per JEDEC JESD47F <sup>††</sup> guidelines)	
Moisture Sensitivity Level	TO-220	N/A
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comment
4/28/2014	<ul style="list-style-type: none"> <li>• Updated data sheet with new IR corporate template.</li> <li>• Updated package outline &amp; part marking on page 7.</li> <li>• Added bullet point in the Benefits "RoHS Compliant, Halogen -Free" on page 1.</li> <li>• Updated typo on the Fig.16 and Fig.17, unit of Y-axis from "A" to "nC" on page 5.</li> </ul>