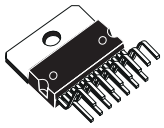
TDA7293

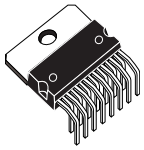
120-volt, 100-watt, DMOS audio amplifier with mute and standby

Features

- Multipower BCD technology
- Very high operating voltage range (±50 V)
- DMOS power stage
- High output power (100 W into 8 Ω @ THD =10%, with V_S = ±40 V)
- Muting and stand-by functions
- No switch on/off noise
- Very low distortion
- Very low noise
- Short-circuit protected (with no input signal applied)
- Thermal shutdown
- Clip detector
- Modularity (several devices can easily be connected in parallel to drive very low impedances)



Multiwatt15V



Multiwatt15H

Description

The TDA7293 is a monolithic integrated circuit in Multiwatt15 package, intended for use as audio class AB amplifier in Hi-Fi field applications, such as home stereo, self powered loudspeakers and Topclass TV. Thanks to the wide voltage range and to the high output current capability it is able to supply the highest power into both 4-Ω and 8-Ω loads.

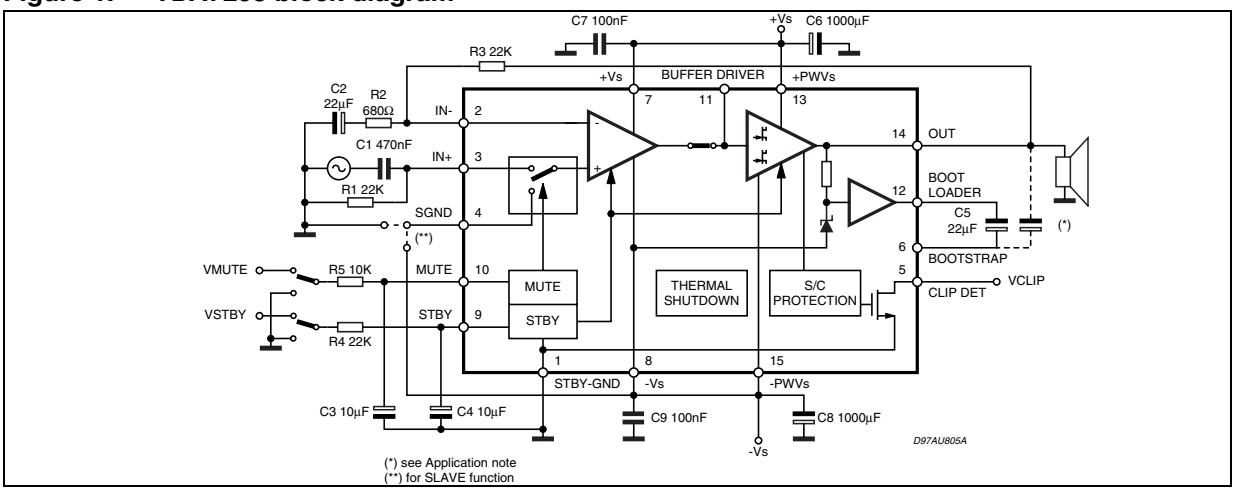
The built-in muting function with turn-on delay simplifies the remote operation avoiding on-off switching noises.

Parallel mode is possible by connecting several devices and using pin11. High output power can be delivered to very low impedance loads, so optimizing the thermal dissipation of the system

Table 1. Device summary

Order code	Package
TDA7293V	Multiwatt15V
TDA7293HS	Multiwatt15H

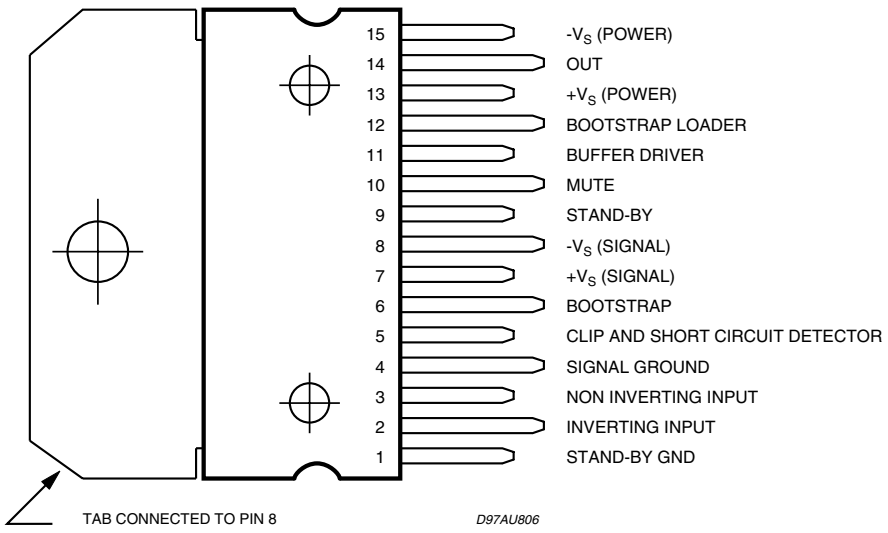
Figure 1. TDA7293 block diagram



Contents

1 Pin connections

Figure 2. Pin connections



2 Electrical specifications

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Supply voltage (no signal)	±60	V
V_1	$V_{STANDBY}$ GND voltage referred to $-V_S$ (pin 8)	90	V
V_2	Input voltage (inverting) referred to $-V_S$	90	V
$V_2 - V_3$	Maximum differential inputs	±30	V
V_3	Input voltage (non inverting) referred to $-V_S$	90	V
V_4	Signal GND voltage referred to $-V_S$	90	V
V_5	Clip detector voltage referred to $-V_S$	120	V
V_6	Bootstrap voltage referred to $-V_S$	120	V
V_9	Standby voltage referred to $-V_S$	120	V
V_{10}	Mute voltage referred to $-V_S$	120	V
V_{11}	Buffer voltage referred to $-V_S$	120	V
V_{12}	Bootstrap loader voltage referred to $-V_S$	100	V
I_O	Output peak current	10	A
P_{tot}	Power dissipation T_{case} = 70°C	50	W
T_{op}	Operating ambient temperature range	0 to 70	°C
T_{stg}, T_j	Storage and junction temperature	150	°C
V_S	Supply voltage (no signal)	±60	V
V_1	$V_{STANDBY}$ GND voltage referred to $-V_S$ (pin 8)	90	V
V_{ESD_HBM}	ESD maximum withstanding voltage range, test condition CDF-AEC-Q100-002- ”Human body model”	±1500	V

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{thj\text{-}case}$	Thermal resistance junction to case	-	1	1.5	°C/W

2.3 Electrical characteristics

The specifications given here were obtained with the conditions V_S = ±40 V, R_L = 8 Ω, R_g = 50 Ω, T_{amb} = 25 °C, f = 1 kHz unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_S	Supply range	-	±12	-	±50	V
I_q	Quiescent current	-	-	50	100	mA
I_b	Input bias current	-	-	0.3	1	µA
V_{OS}	Input offset voltage	-	-10	-	10	mV
I_{OS}	Input offset current	-	-	-	0.2	µA
P_O	Continuous output power	d = 1%, R_L = 4 Ω, V_S = ±29 V	75	80 80	-	W
		d = 10%, R_L = 4Ω, V_S = ±29 V	90	100 100	-	W
d	Total harmonic distortion (1)	P_O = 5 W, f = 1 kHz	-	0.005	-	%
		P_O = 0.1 to 50 W, f = 20 Hz to 15 kHz	-	-	0.1	%
I_{SC}	Current limiter threshold	$V_S \leq$ ±40 V	-	6.5	-	A
SR	Slew rate	-	5	10	-	V/µs
G_V	Open loop voltage gain	-	-	80	-	dB
G_V	Closed loop voltage gain (2)	-	29	30	31	dB
e_N	Total input noise	A = curve	-	1	-	µV
		f = 20 Hz to 20 kHz	-	3	10	µV
R_i	Input resistance	-	100	-	-	kΩ
SVR	Supply voltage rejection	f = 100 Hz, V_{ripple} = 0.5 V RMS	-	75	-	dB
T_S	Thermal protection	Device mutes	-	150	-	°C
		Device shuts down	-	160	-	°C
Standby function (ref. to to pin 1)						
$V_{ST\ on}$	Standby on threshold	-	-	-	1.5	V
$V_{ST\ off}$	Standby off threshold	-	3.5	-	-	V
$ATT_{st\text{-}by}$	Standby attenuation	-	70	90	-	dB
$I_{q\ st\text{-}by}$	Quiescent current @ standby	-	-	0.5	1	mA
Mute function (ref. to pin 1)						
V_{Mon}	Mute on threshold	-	-	-	1.5	V
V_{Moff}	Mute off threshold	-	3.5	-	-	V
ATT_{mute}	Mute attenuatIon	-	60	80	-	dB

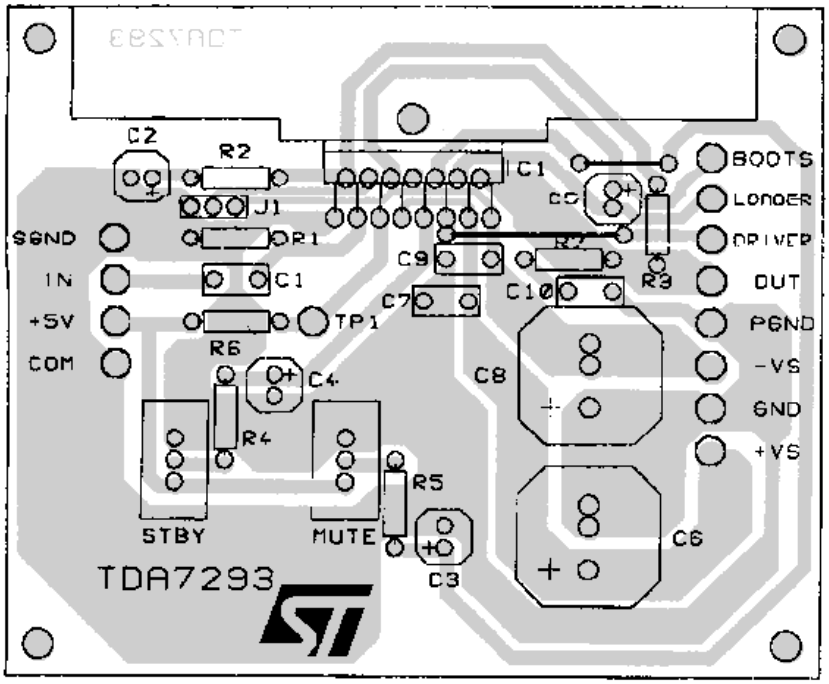
Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Clip detector						
Duty	Duty cycle (pin 5)	d = 1%, R_{PULLUP} = 10 kΩ to 5 V	-	10	-	%
		d = 10%, R_{PULLUP} = 10 kΩ to 5 V	30	40	50	%
I_{CLEAK}	-	P_O = 50 W	-	-	3	µA
Slave function pin 4 (ref. to pin 8)						
V_{Slave}	Slavethreshold	-	-	-	1	V
V_{Master}	Master threshold	-	3	-	-	V

1. Tested with optimized applications board (see fig. 3)
2. $G_{Vmin} \geq 26dB$

Note: Pin 11 only for modular connection. Max external load 1 MΩ / 10 pF, only for test purposes

Figure 3. Typical application PCB and component layout



3 Circuit description

In consumer electronics, an increasing demand has arisen for very high power monolithic audio amplifiers able to match, with a low cost, the performance obtained from the best discrete designs.

The task of realizing this linear integrated circuit in conventional bipolar technology is made extremely difficult by the occurence of 2nd breakdown phoenomenon. It limits the safe operating area (SOA) of the power devices, and, as a consequence, the maximum attainable output power, especially in presence of highly reactive loads.

Moreover, full exploitation of the SOA translates into a substantial increase in circuit and layout complexity due to the need of sophisticated protection circuits.

To overcome these substantial drawbacks, the use of power MOS devices, which are immune from secondary breakdown is highly desirable.

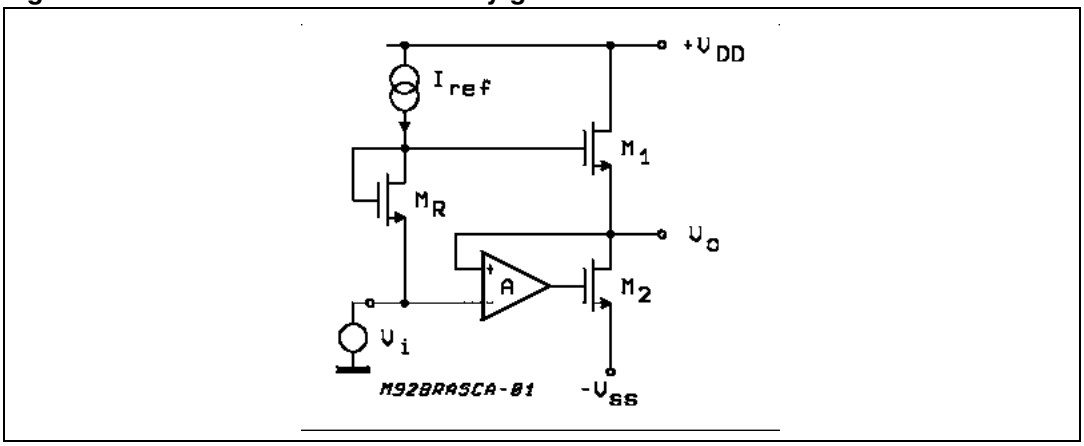
The device described has therefore been developed in a mixed bipolar-MOS high voltage technology called BCDII 100/120.

3.1 Output Stage

The main design task in developping a power operational amplifier, independently of the technology used, is that of realization of the output stage.

The solution shown as a principle shematic by Fig6 represents the DMOS unity - gain output buffer of the TDA7293.

Figure 4. Schematic of a DMOS unity-gain buffer



This large-signal, high-power buffer must be capable of handling extremely high current and voltage levels while maintaining acceptably low harmonic distortion and good behaviour over frequency response; moreover, an accurate control of quiescent current is required.

A local linearizing feedback, provided by differential amplifier A, is used to fullfil the above requirements, allowing a simple and effective quiescent current setting. Proper biasing of the power output transistors alone is however not enough to guarantee the absence of crossover distortion.

While a linearization of the DC transfer characteristic of the stage is obtained, the dynamic behaviour of the system must be taken into account.

A significant aid in keeping the distortion contributed by the final stage as low as possible is provided by the compensation scheme, which exploits the direct connection of the Miller capacitor at the amplifier's output to introduce a local AC feedback path enclosing the output stage itself.

3.2 Protection

In designing a power IC, particular attention must be reserved to the circuits devoted to protection of the device from short circuit or overload conditions. Due to the absence of the 2nd breakdown phenomenon, the SOA of the power DMOS transistors is delimited only by a maximum dissipation curve dependent on the duration of the applied stimulus.

In order to fully exploit the capabilities of the power transistors, the protection scheme implemented in this device combines a conventional SOA protection circuit with a novel local temperature sensing technique which " dynamically" controls the maximum dissipation.

In addition to the overload protection described above, the device features a thermal shutdown circuit which initially puts the device into a muting state (@ $T\varphi$ = 150 °C) and then into stand-by (@ T_j = 160 °C).

Full protection against electrostatic discharges on very pin is included.

3.3 Other Features

The device is provided with both standby and mute functions, independently driven by two CMOS logic compatible input pins.

The circuits dedicated to the switching on and off of the amplifier have been carefully optimized to avoid any kind of uncontrolled audible transient at the output.

The sequence that we recommend during the on/off transients is shown in Figure 8. The application of figure 9 shows the possibility of sing only one command for both st-by and mute functions. On both the pins, the maximum applicable range corresponds to the operating supply voltage.

Figure 5. Suggested turn-on/off sequence

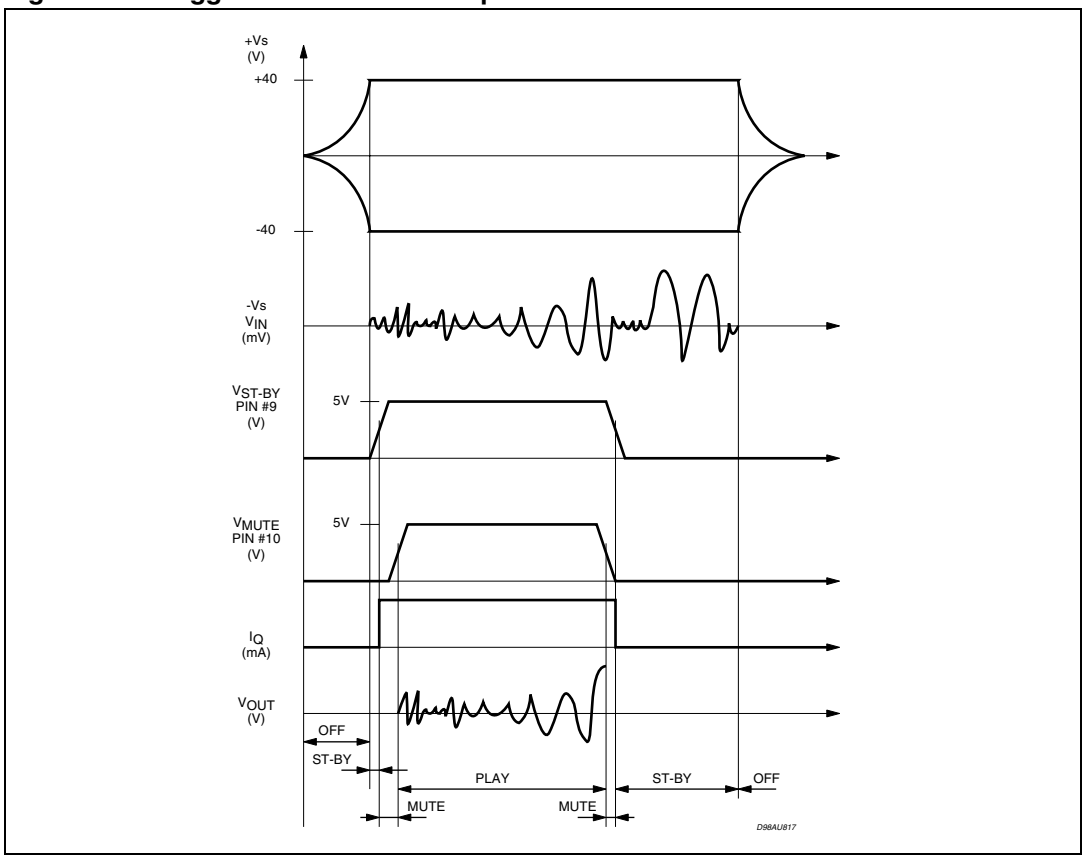
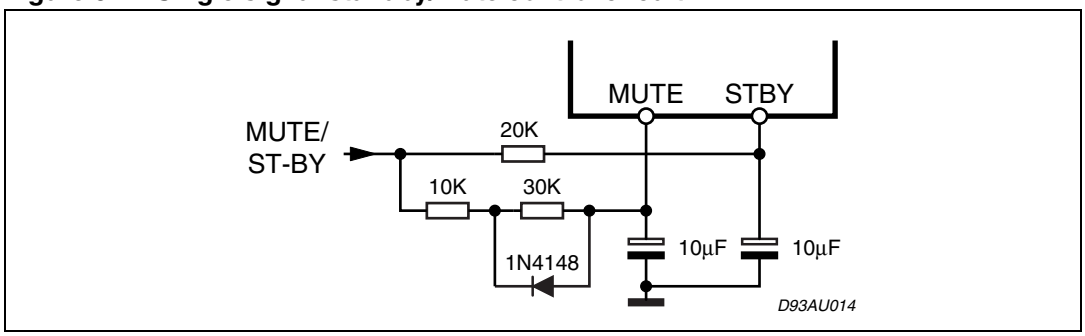


Figure 6. Single signal standby/mute control circuit



4 Applications information

4.1 Applications suggestions

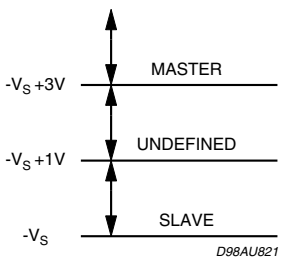
The recommended values of the external components are those shown on the application circuit of *Figure 1 on page 1*. Different values can, however, be used and the following table could be useful when choosing alternative values.

Table 5. Choosing alternative component values

Component	Suggested value	Purpose	Larger than suggested	Smaller than suggested
R1 (1)	22 kΩ	Input resistance	Increase input impedance	Decrease input impedance
R2	680 Ω	Closed loop gain, set to 30 dB (2)	Decrease of gain	Increase of gain
R3 (1)	22 kΩ		Increase of gain	Decrease of gain
R4	22 kΩ	Standby time constant	Larger Standby on/off time	Smaller standby ON/OFF time; pop noise
R5	10 kΩ	Mute time constant	Larger mute on/off time	Smaller mute on/off time
C1	0.47 µF	Input DC decoupling	-	Higher low-frequency cutoff
C2	22 µF	Feedback DC decoupling	-	Higher low-frequency cutoff
C3	10 µF	Mute time constant	Larger mute on/off time	Smaller mute on/off time
C4	10 µF	Standby time constant	Larger standby on/off time	Smaller standby on/off time; pop noise
C5	22 µF (3) x N	Bootstrapping	-	Signal degradation at low frequency
C6, C8	1000 µF	Supply voltage bypass	-	-
C7, C9	0.1 µF	Supply voltage bypass	-	Danger of oscillation

1. R1 = R3 for pop optimization
2. Closed loop gain has to be ³ 26dB
3. Multiply this value by the number, N, of modular parts connected

Figure 7. Slave function: pin 4 (Ref to pin 8)



Note: If in the application the speakers are connected via long wires, it is a good rule to add, between the output and GND, a boucherot cell in order to avoid dangerous spurious oscillations if the speakers terminal are shorted.
The suggested boucherot resistor is 3.9Ω/2W and the capacitor is 1µF.

4.2 High efficiency

Constraints of implementing high power solutions are the power dissipation and the size of the power supply. These are both due to the low efficiency of conventional AB class amplifier approaches.

The circuit below in *Figure 8* is a high efficiency amplifier which can be adopted for both hi-fi and car-radio applications. The TDA7293 is a monolithic MOS power amplifier which can be operated with a 100-V supply (120 V with no signal applied) while delivering output currents up to ±6.5 A. This allows the use of this device as a very high-power amplifier (up to 180 W peak power with THD = 10% and R_L = 4 Ω); the only drawback is the power dissipation, hardly manageable in the above power range.

The typical junction-to-case thermal resistance of the TDA7293 is 1 °C/W (max = 1.5 °C/W). In worst case conditions, to avoid the chip temperature exceeding 150 °C the thermal resistance of the heatsink must be 0.038 °C/W (at a maximum ambient temperature of 50 °C).

As the above value is pratically unreachable, a high efficiency system is needed in those cases where the continuous average output power is higher than 50 to 60 W.

The TDA7293 was designed to work also in a higher efficiency way. For this reason there are four power supply pins: two intended for the signal part and two for the power part. T1 and T2 are two power transistors that only operate when the output power reaches a certain threshold (for example, 20 W).

If the output power increases, these transistors are switched on during the portion of the signal where more output voltage swing is needed, thus "bootstrapping" the power supply pins (13 and 15). The current generators formed by T4, T7, zener diodes Z1, Z2 and resistors R7, R8 define the minimum drop across the power MOS transistors of the TDA7293. L1, L2, L3 and the snubbers C9, R1 and C10, R2 stabilize the loops formed by the "bootstrap" circuits and the output stage of the TDA7293.

By considering again a maximum average output power (music signal) of 20 W, in case of the high efficiency application, the thermal resistance value needed from the heatsink is 2.2 °C/W (with V_S = ±50 V and R_L = 8 Ω). All components (TDA7293 and power transistors T1 and T2) can be placed on a 1.5 °C/W heatsink, with the power darlingtons electrically insulated from the heatsink.

Since the total power dissipation is less than that of a usual class AB amplifier, additional cost savings can be obtained while optimizing the power supply, even with a large heatsink.

4.3 Bridge application

Another application suggestion is the bridge configuration, where two TDA7293 are used.

In this application, the value of the load must not be lower than 8 Ω for dissipation and current capability reasons.

A suitable field of application includes hi-fi/TV subwoofer realizations. The main advantages offered by this solution are:

- High power performance with limited supply voltage level.
- Considerably higher output power even with high load values, such as 16 Ω.

With R_L = 8 Ω and V_S = ±25 V, the maximum output power obtainable is 150 W, whilst with R_L = 16 Ω and V_S = ±40 V, the maximum Pout is 200 W.

4.4 Modular application (ref. figure 12)

The modular application is where several devices operate in parallel.

The modular application allows very high power be delivered to very low-impedance loads. In this type of application one device acts as a master and the others as slaves.

The slave power stages are driven by the master device and work in parallel together while the input and the gain stages of the slave devices are disabled. The figure below shows the connections required to configure two devices to work together.

- The master chip connections are the same as the normal single ones.
- The outputs can be connected together **without the need of any ballast resistor**.
- The slave SGND pin must be tied to the negative supply.
- The slave STANDBY and MUTE pins must be connected to the master STANDBY and MUTE pins.
- The bootstrap lines must be connected together and the bootstrap capacitor must be increased: for N devices the bootstrap capacitor must be 22 µF times N.
- The slave IN pin must be connected to the negative supply.

4.5 Bootstrap capacitor

For compatibility purpose with the previous devices of the family, the bootstrap capacitor can be connected either between the bootstrap pin (6) and the output pin (14) or between the bootstrap pin (6) and the bootstrap loader pin (12).

When the bootstrap is connected between pins 6 and 14 the maximum supply voltage in the presence of an output signal is limited to 100 V, due the bootstrap capacitor overvoltage.

When the bootstrap is connected between pins 6 and 12 the maximum supply voltage extends to the full voltage that the technology can stand, in this case 120 V.

This is accomplished by the clamp introduced at the bootstrap loader pin (12). This pin follows the output voltage up to 100 V and remains clamped at 100 V for higher output voltages.

This feature lets the output voltage swing up to a gate-source voltage from the positive supply (V_S -3 to 6 V).

Figure 8. High-efficiency applications circuit

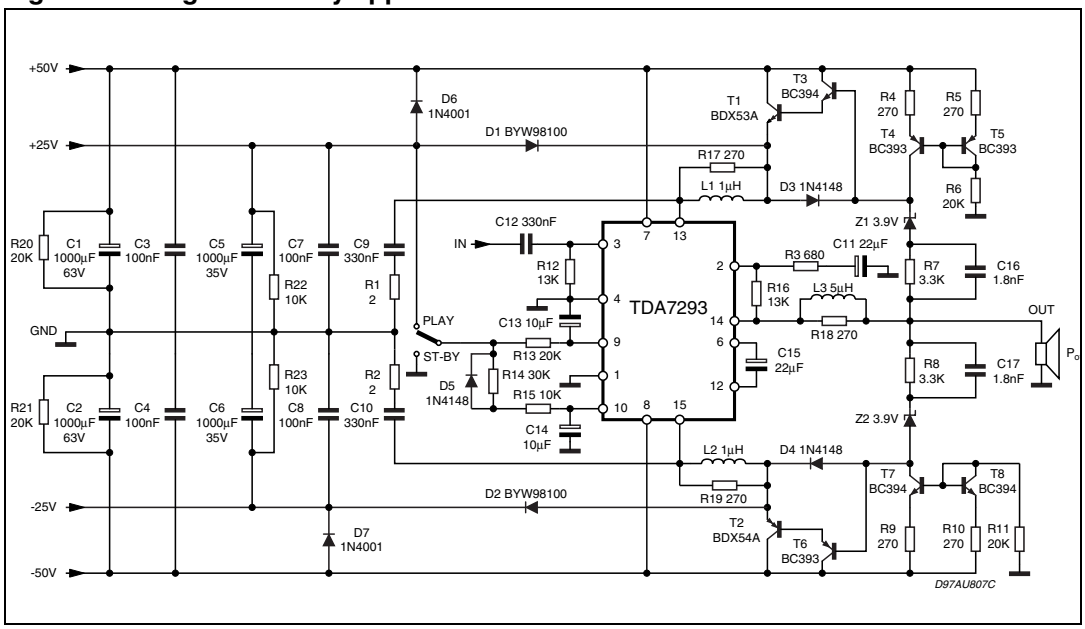


Figure 9. PCB and component layout of fig. 8

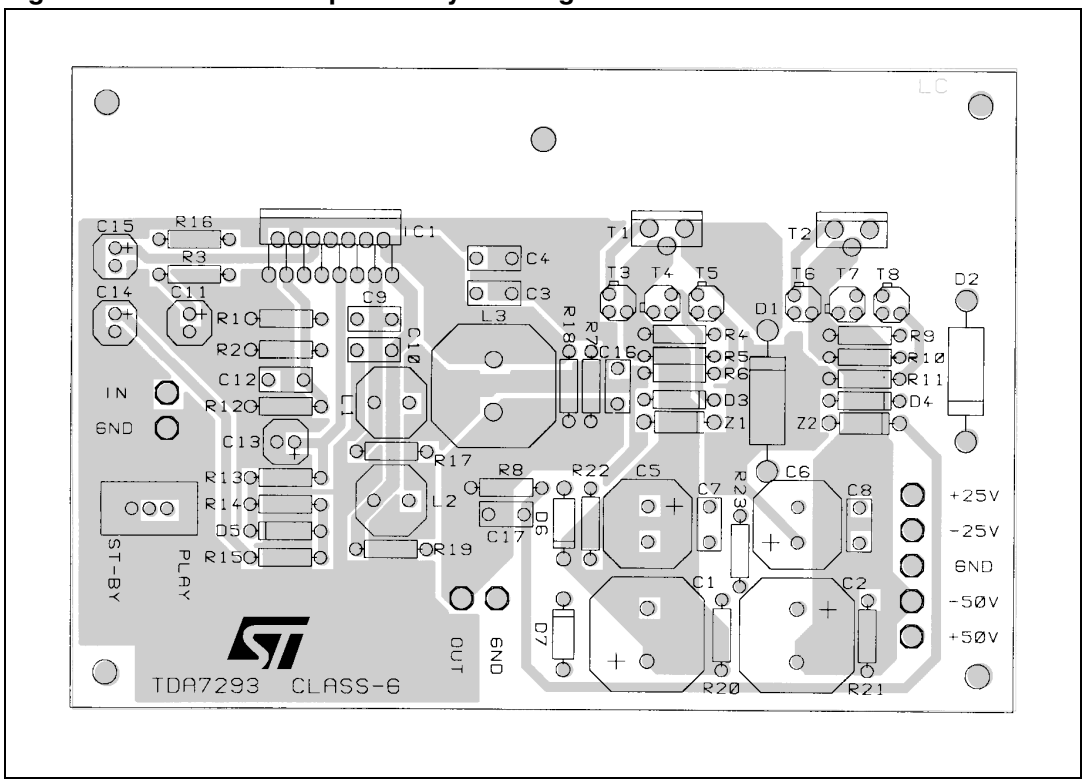


Figure 10. PCB - solder side of the Fig 9

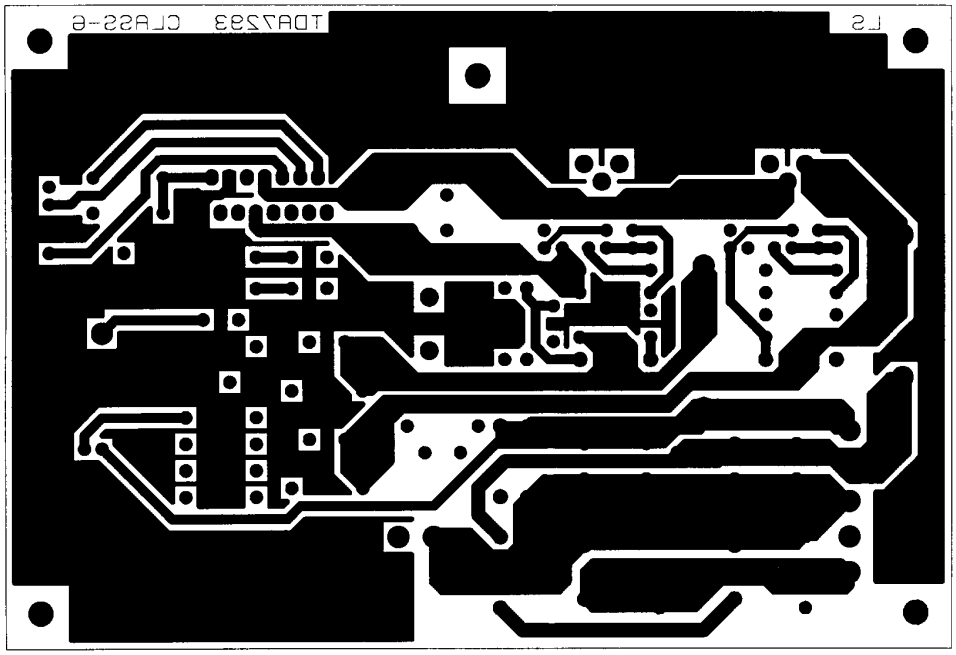


Figure 11. Modular application circuit

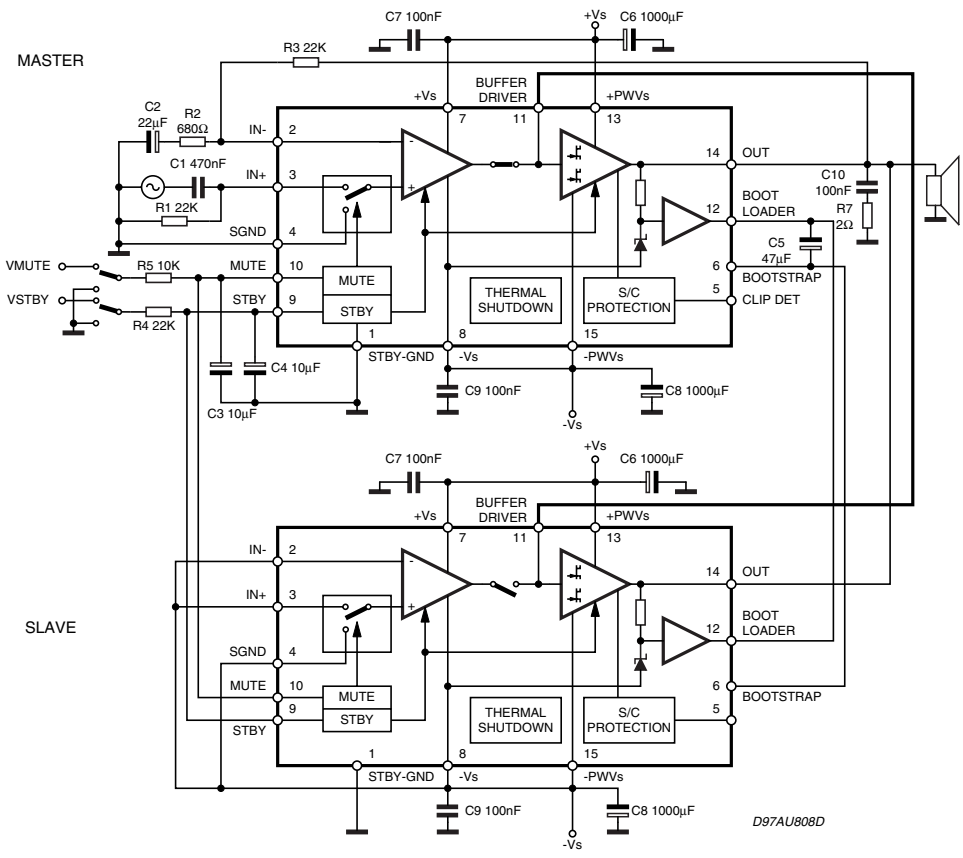


Figure 12. Modular application PCB and component layout (component side)

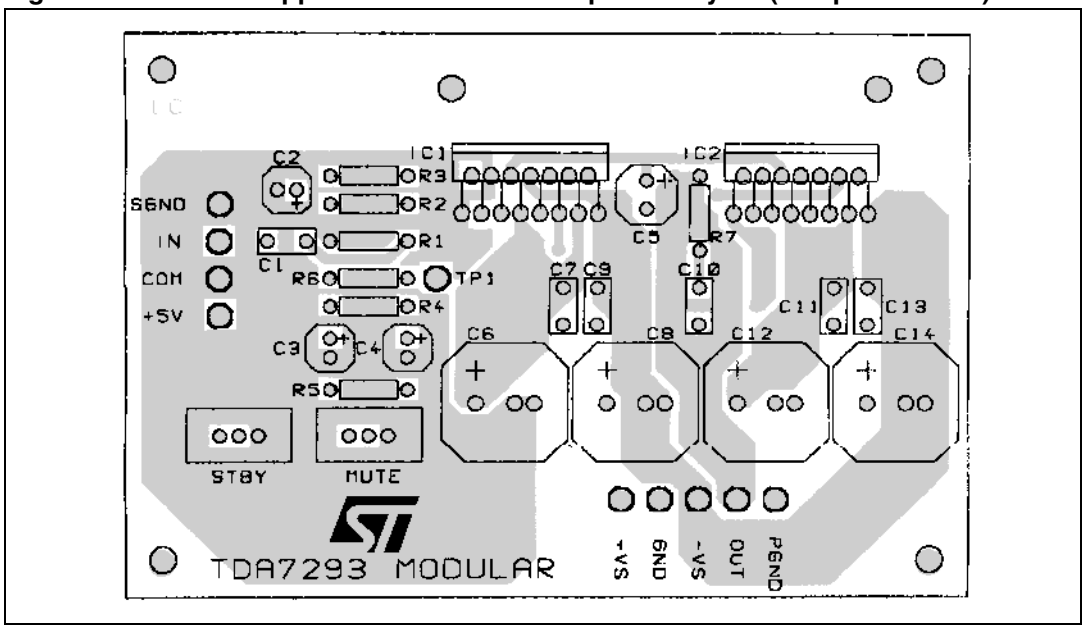


Figure 13. Modular application PCB and component layout (solder side)

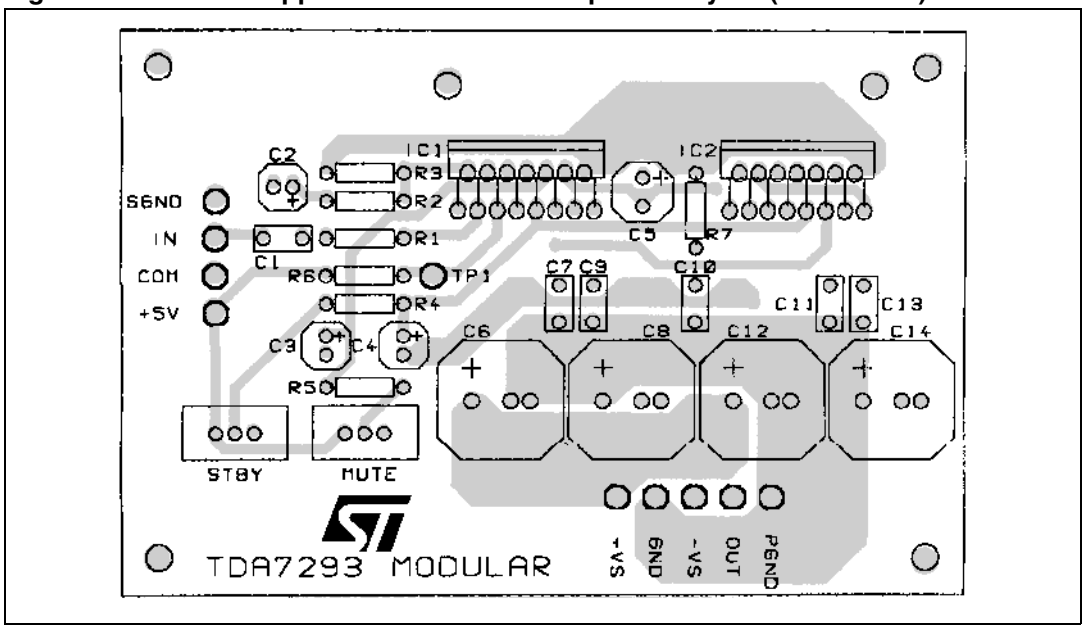


Figure 14. Distortion vs output power

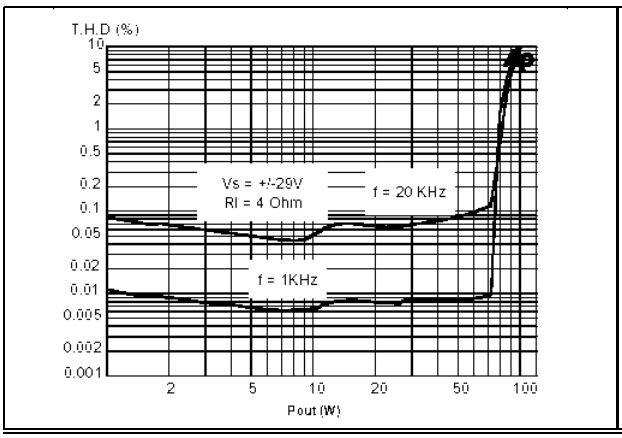


Figure 15. Distortion vs output power

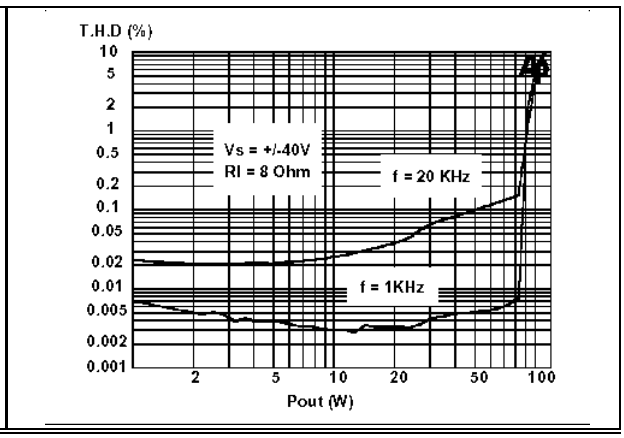


Figure 16. Distortion vs frequency

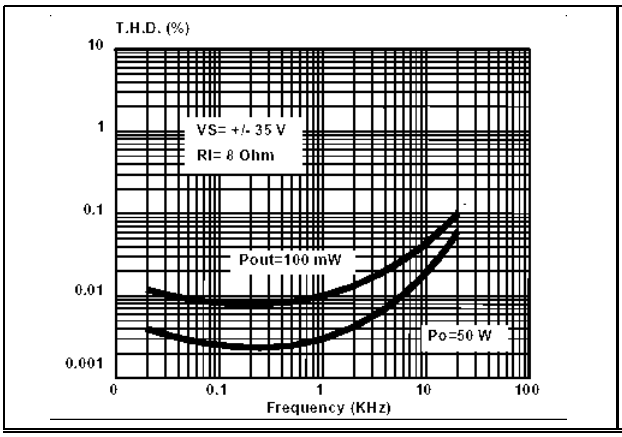


Figure 17. Modular application derating rload vs voltage supply (ref. fig. 12)

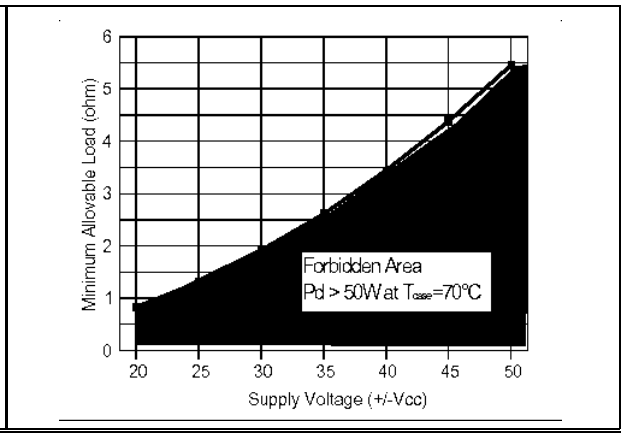


Figure 18. Modular application Pd vs voltage supply (ref. fig. 12)

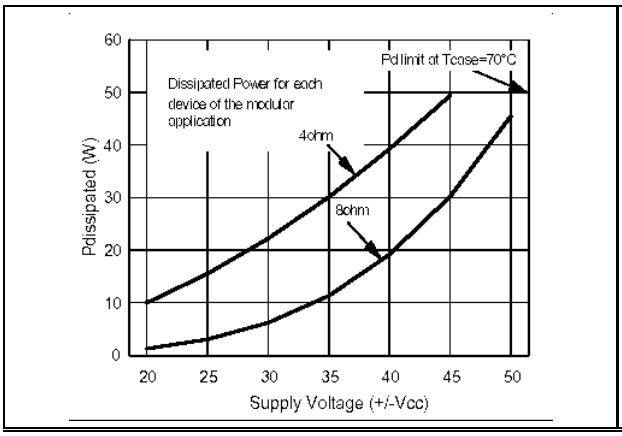
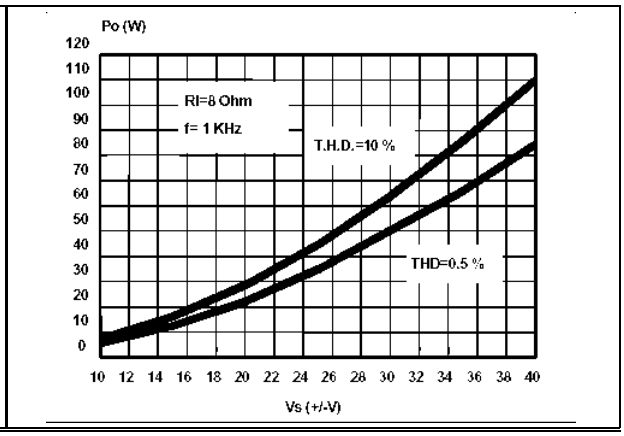


Figure 19. Output power vs. supply voltage



5 Package mechanical data

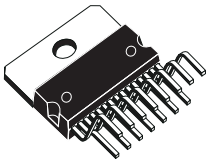
The TDA7293 comes with a choice of two 15-pin packages, Multiwatt15V and Multiwatt15H. The package sizes and outline drawings are given below.

5.1 Vertically-mounted package

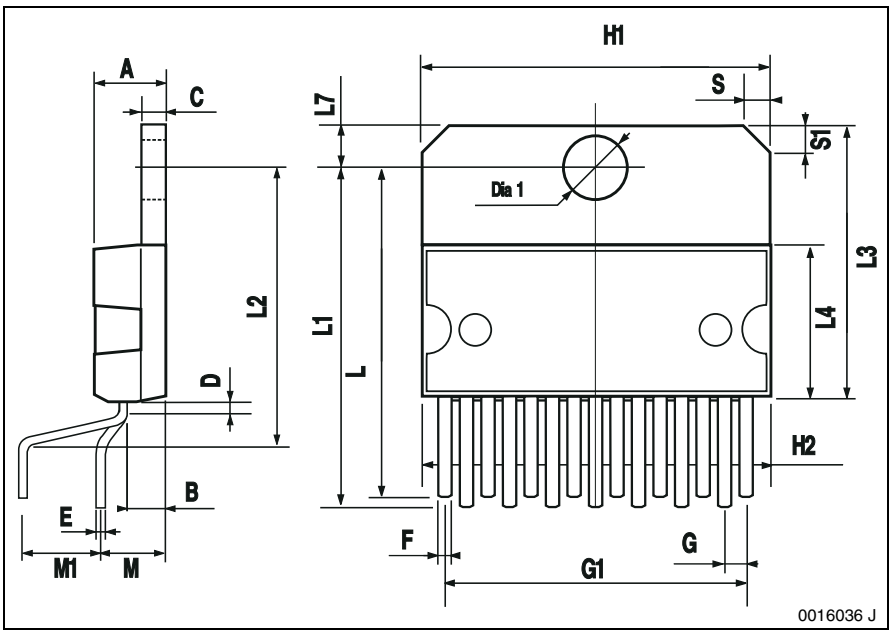
Figure 20. Multiwatt15V package

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A5						0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.87	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.73	5.08	5.43	0.186	0.200	0.214
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



Multiwatt15 (Vertical)



5.2 Horizontally-mounted package

Figure 21. Multiwatt15H outline

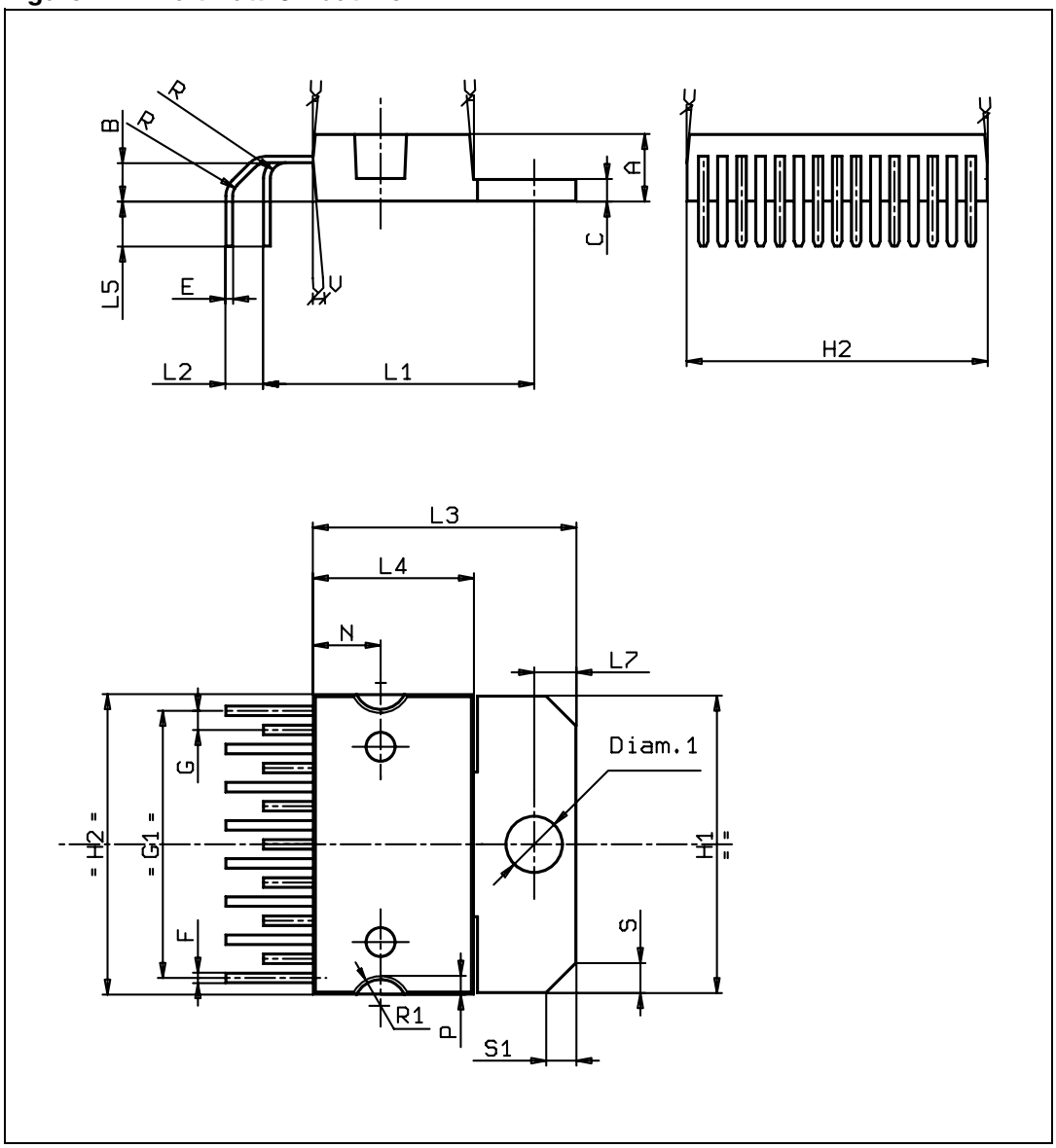


Table 6. Multiwatt15H dimensions

Ref	Dimension in mm			Dimension in inch			Notes
	Min	Typ	Max	Min	Typ	Max	
A	-	-	5.00	-	-	0.197	-
B	-	-	2.65	-	-	0.104	-
C	-	-	1.60	-	-	0.063	-
E	0.49	-	0.55	0.019	-	0.022	-
F	0.66	-	0.75	0.026	-	0.030	-
G	1.02	1.27	1.52	0.040	0.050	0.060	-
G1	17.53	17.78	18.03	0.690	0.700	0.710	-
H1	19.60	-	20.20	0.772	-	0.795	-
H2	19.60	-	20.20	0.772	-	0.795	-
L1	17.80	18.00	18.20	0.701	0.709	0.717	-
L2	2.30	2.50	2.80	0.091	0.098	0.110	-
L3	17.25	17.50	17.75	0.679	0.689	0.699	-
L4	10.30	10.70	10.90	0.406	0.421	0.429	-
L5	2.70	3.00	3.30	0.106	0.118	0.130	-
L7	2.65	-	2.90	0.104	-	0.114	-
N	-	-	-	-	-	-	-
P	-	-	-	-	-	-	-
R	-	1.50	-	-	0.059	-	-
R1	-	-	-	-	-	-	-
S	1.90	-	2.60	0.075	-	0.102	-
S1	1.90	-	2.60	0.075	-	0.102	-
V	-	-	-	-	-	-	-
Diam.1	3.65	-	3.85	0.144	-	0.152	-

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

6 Revision history

Table 7. Document revision history

Date	Revision	Changes
Jan-2004	7	First Issue in EDOCS
Aug-2004	7.1	Stylesheet update. No content change
24-Sep-2010	8	Updated package dimensions for Multiwatt15H in *Table 6 on page 19* Updated presentation throughout document.