



UCx52xA Regulating Pulse Width Modulators

1 Features

- 8-V to 35-V Operation
- 5.1-V Reference Trimmed to 1%
- 100-Hz to 500-kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Dead-Time Control
- Internal Soft Start
- Pulse-by-Pulse Shutdown
- Input Undervoltage Lockout With Hysteresis
- Latching PWM to Prevent Multiple Pulses
- Dual Source and Sink Output Drivers

2 Applications

- Off-Line and DC/DC Power Supplies
- Converters Using Voltage Mode
- Single-Ended or Two-Switch Topology Designs
- Solar Inverters
- Welding Inverters
- Motor Control
- Battery Chargers

3 Description

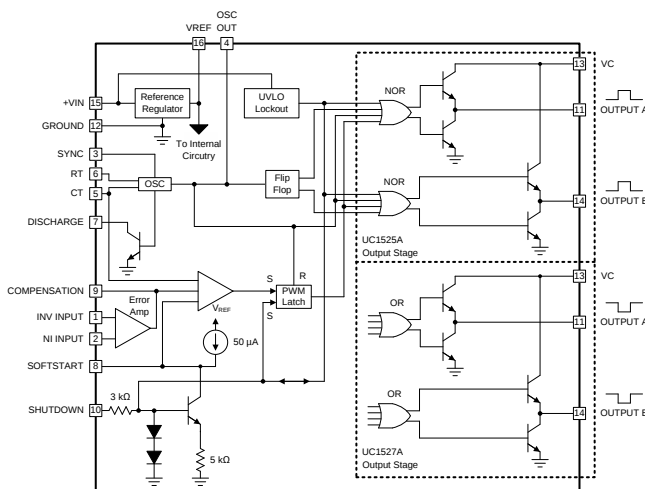
The UC1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip 5.1-V reference is trimmed to 1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between C_T and the discharge terminals provides a wide range of dead-time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCx52xA	LCCC (20)	8.89 mm × 8.89 mm
	CDIP (16)	19.56 mm × 6.67 mm
	SOIC (16)	10.30 mm × 7.50 mm
	PDIP (16)	19.30 mm × 6.35 mm
	PLCC (20)	8.96 mm × 8.96 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



Copyright © 2017, Texas Instruments Incorporated



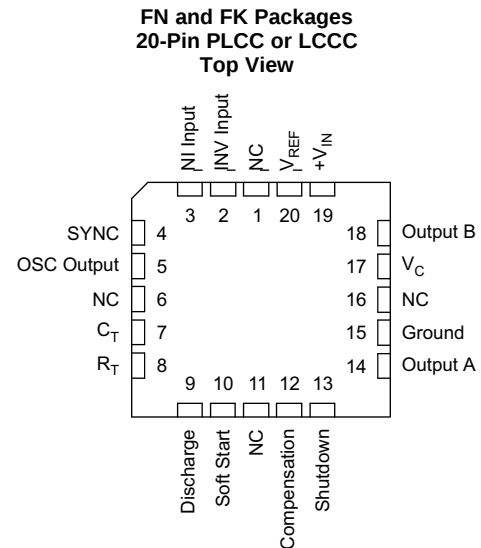
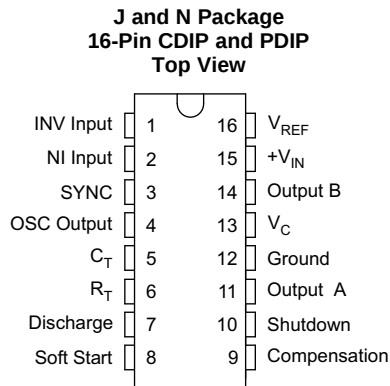
Table of Contents

1 Features	1	7.4 Device Functional Modes.....	9
2 Applications	1	8 Application and Implementation	10
3 Description	1	8.1 Application Information.....	10
4 Revision History	2	8.2 Typical Application	10
5 Pin Configuration and Functions	3	9 Power Supply Recommendations	16
6 Specifications	4	10 Layout	16
6.1 Absolute Maximum Ratings	4	10.1 Layout Guidelines	16
6.2 ESD Ratings.....	4	10.2 Layout Example	16
6.3 Recommended Operating Conditions.....	4	11 Device and Documentation Support	17
6.4 Thermal Information	5	11.1 Documentation Support	17
6.5 Electrical Characteristics.....	5	11.2 Related Links	17
6.6 Typical Characteristics	7	11.3 Community Resources.....	17
7 Detailed Description	8	11.4 Trademarks	17
7.1 Overview	8	11.5 Electrostatic Discharge Caution.....	17
7.2 Functional Block Diagram	8	11.6 Glossary	17
7.3 Feature Description.....	9	12 Mechanical, Packaging, and Orderable Information	17

4 Revision History

Changes from Revision C (January 2008) to Revision D	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Added <i>Thermal Information</i> table	5
• Changed $R_{\theta JA}$ values in the <i>Thermal Information</i> table: from 80-120 to N/A for J; from 90 to 47.6 for N; from 45-90 to 72.6 for DW; from 43-75 to 55.8 for FN; and from 70-80 to N/A for FK	5
• Changed $R_{\theta JC}$ values in the <i>Thermal Information</i> table: from 28 to 37.4 (top) and 10.1 (bottom) for J; from 45 to 37.3 (top) for N; from 25 to 34 (top) for DW; from 34 to 33.7 (top) for FN; and from 20 to 32.9 (top) to 3.5 (bottom) for FK	5

5 Pin Configuration and Functions



Pin Functions

PIN			I/O	DESCRIPTION
NAME	CDIP, PDIP	PLCC, LCCC		
INV Input	1	2	I	Inverting input to the error amplifier
NI Input	2	3	I	Noninverting input to the error amplifier
SYNC	3	4	I	Oscillator sync terminal
OSC Output	4	5	O	Oscillator frequency output
CT	5	7	I	Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length.
RT	6	8	I	Timing resistor connection pin for oscillator frequency programming
Discharge	7	9	I	A single resistor between CT and the discharge terminals provides dead-time adjustment
Soft Start	8	10	I	Soft-start input pin.
Compensation	9	12	O	Output of the error amplifier for compensation
Shutdown	10	13	I	Pull this pin high to shut down PWM output
Output A	11	14	O	output A of the on-chip drive stage
Ground	12	15	—	Ground return pin
VC	13	17	—	Power supply pin for the output stage. This pin should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths.
Output B	14	18	O	Output B of the on-chip drive stage.
+VIN	15	19	—	Input voltage
VREF	16	20	O	5.1-V reference. For stability, the reference should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane.
NC	—	1, 6, 11, 16	—	No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
+V _{IN}	Supply voltage		40	V
V _C	Collector supply voltage		40	V
	Logic inputs	–0.3	5.5	V
	Analog inputs	–0.3	+V _{IN}	V
	Output current, source or sink		500	mA
	Reference output current		50	mA
	Oscillator charging current		5	mA
	Power dissipation at T _A = +25°C(2)		1000	mW
	Power dissipation at T _C = +25°C(2)		2000	mW
	Operating junction temperature	–55	150	°C
	Lead temperature (soldering, 10 seconds)		300	°C
T _{stg}	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	3000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
+V _{IN}	Input voltage	8	35	V
V _C	Collector supply voltage	4.5	35	V
	Sink/source load current (steady state)	0	100	mA
	Sink/source load current (peak)	0	400	mA
	Reference load current	0	20	mA
	Oscillator frequency range	100	400	Hz
	Oscillator timing resistor	2	150	kΩ
	Oscillator timing capacitor	0.001	0.01	μF
	Dead time resistor range	0	500	Ω
Operating ambient temperature	UC1525A, UC1527A	–55	125	°C
	UC2525A, UC2527A	–25	85	
	UC3525A, UC3527A	0	70	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		UCx52xA					UNIT
		FK (LCCC)	J (CDIP)	DW (SOIC)	N (PDIP)	FN (PLCC)	
		20 PINS	16 PINS	16 PINS	16 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	N/A	N/A	72.6	47.6	55.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	32.9	37.4	34	37.3	33.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	32.1	54.2	37.3	27.7	21.1	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	N/A	N/A	8.9	17.3	9.7	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	N/A	N/A	36.8	27.5	20.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	3.5	10.1	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE						
Output voltage	T _J = 25°C	UC152xA, UC252xA	5.05	5.1	5.15	V
		UC352xA	5	5.1	5.2	
Line regulation	V _{IN} = 8 V to 35 V		10		20	mV
Load regulation	I _L = 0 mA to 20 mA		20		50	mV
Temperature stability ⁽¹⁾	Over operating		20		50	mV
Total output variation ⁽¹⁾	Line, load, and temperature	UC152xA, UC252xA	5		5.2	V
		UC352xA	4.95		5.25	
Shorter circuit current	V _{REF} = 0, T _J = 25°C		80		100	mA
Output noise Voltage ⁽¹⁾	10 Hz ≤ 10 kHz, T _J = 25°C		40		200	μVrms
Long-term stability ⁽¹⁾	T _J = 125°C		20		50	mV
OSCILLATOR SECTION ⁽²⁾						
Initial accuracy ⁽¹⁾⁽²⁾	T _J = 25°C		2%		6%	
Voltage stability ⁽¹⁾⁽²⁾	V _{IN} = 8 V to 35 V	UC152xA, UC252xA	0.3%		1%	
		UC352xA	1%		2%	
Temperature stability ⁽¹⁾	Over operating		3%		6%	
Minimum frequency	R _T = 200 kΩ, C _T = 0.1 mF				120	Hz
Maximum frequency	R _T = 2 kΩ, C _T = 470 pF		400			kHz
Current mirror	I _{RT} = 2 mA		1.7	2	2.2	mA
Clock amplitude ⁽¹⁾⁽²⁾			3	3.5		V
Clock width ⁽¹⁾⁽²⁾	T _J = 25°C		0.3	0.5	1	μs
Synchronization threshold ⁽¹⁾⁽²⁾			1.2	2	2.8	V
Sync input current	Sync voltage = 3.5 V		1		2.5	mA
ERROR AMPLIFIER SECTION (V _{CM} = 5.1 V)						
Input offset voltage	UC152xA, UC252xA		0.5		5	mV
	UC352xA		2		10	

(1) These parameters, although ensured over the recommended operating conditions, are not 100% tested in production.

(2) Tested at f_{OSC} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 mF, R_D = 0. Approximate oscillator frequency is defined by

$$f = \frac{1}{C_T (0.7R_T + 3R_D)}$$

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input bias current			1	10	μA
Input offset current				1	
DC open loop gain	R _L ≥ 10 MΩ	60	75		dB
Gain-bandwidth product ⁽¹⁾	A _V = 0 dB, T _J = 25°C	1	2		MHz
DC transconductance ⁽¹⁾⁽³⁾	T _J = 25°C, 30 kΩ ≤ R _L ≤ 1 MΩ	1.1	1.5		mS
Low-level output voltage			0.2	0.5	V
High-level output voltage		3.8	5.6		
Common mode rejection	V _{CM} = 1.5 V to 5.2 V	60	75		dB
Supply voltage rejection	V _{IN} = 8 V to 35 V	50	60		
PWM COMPARATOR					
Minimum duty-cycle				0%	
Maximum duty-cycle		45%	49%		
Input threshold ⁽⁴⁾	Zero duty-cycle	0.7	0.9		V
	Maximum duty-cycle		3.3	3.6	
Input bias current ⁽⁴⁾			0.05	1	μA
SHUTDOWN					
Soft-start current	V _{SD} = 0 V, V _{SS} = 0 V	25	50	80	μA
Soft-start low level	V _{SD} = 2.5 V		0.4	0.7	V
Shutdown threshold	To outputs, V _{SS} = 5.1 V, T _J = 25°C	0.6	0.8	1	
Shutdown input current	V _{SD} = 2.5 V		0.4	1	mA
Shutdown Delay ⁽⁵⁾	V _{SD} = 2.5 V, T _J = 25°C		0.2	0.5	μS
OUTPUT DRIVERS (EACH OUTPUT) (V _C = 20 V)					
Low-level output voltage	I _{SINK} = 20 mA		0.2	0.4	V
	I _{SINK} = 100 mA		1	2	
High-level output voltage	I _{SOURCE} = 20 mA	18	19		V
	I _{SOURCE} = 100 mA	17	18		
Undervoltage lockout	V _{COMP} and V _{SS} = High	6	7	8	V
V _C OFF current ⁽⁶⁾	V _C = 35 V			200	μA
Rise time ⁽⁵⁾	C _L = 1 nF, T _J = 25°C		100	600	ns
Fall time ⁽⁵⁾	C _L = 1 nF, T _J = 25°C		50	300	
TOTAL STANDBY CURRENT					
Supply current	V _{IN} = 35 V		14	20	mA

(3) DC transconductance (g_M) relates to DC open-loop voltage gain (A_V) according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.

(4) Tested at $f_{OSC} = 40 \text{ kHz}$ ($R_T = 3.6 \text{ k}\Omega$, $C_T = 0.01 \text{ mF}$, $R_D = 0 \Omega$).

(5) These parameters, although ensured over the recommended operating conditions, are not 100% tested in production.

(6) Collector off-state quiescent current measured at pin 13 with outputs low for UC1525A and high for UC1527A.

6.6 Typical Characteristics

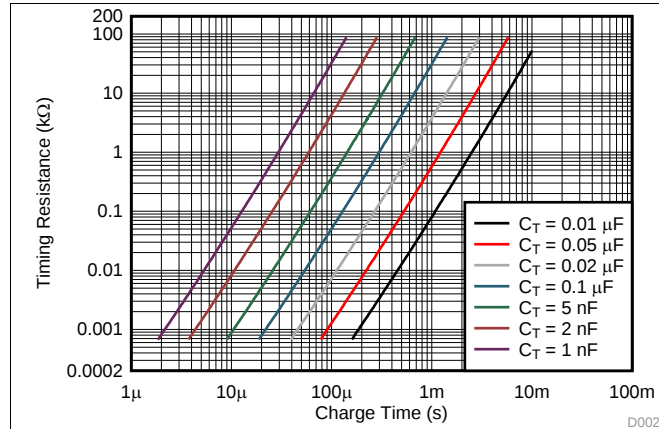


Figure 1. Oscillator Charge Time vs R_T and C_T

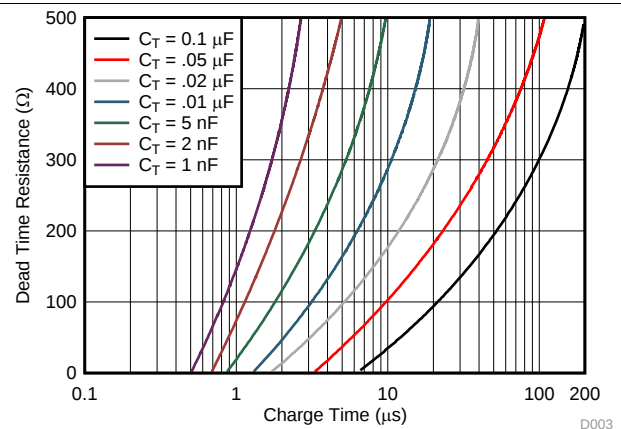


Figure 2. Oscillator Discharge Time vs R_T C_T

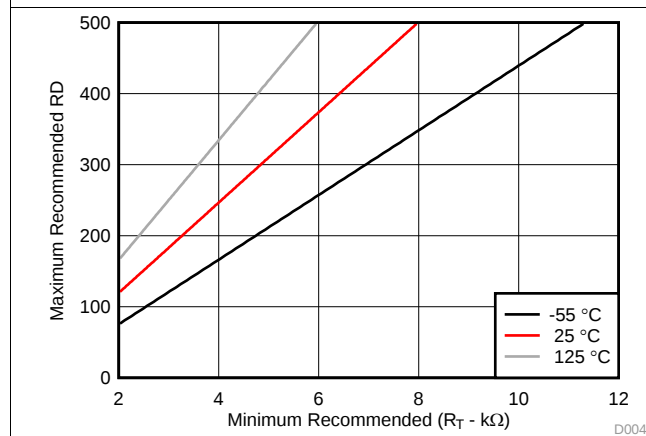


Figure 3. Maximum Value R_D vs Minimum Value R_T

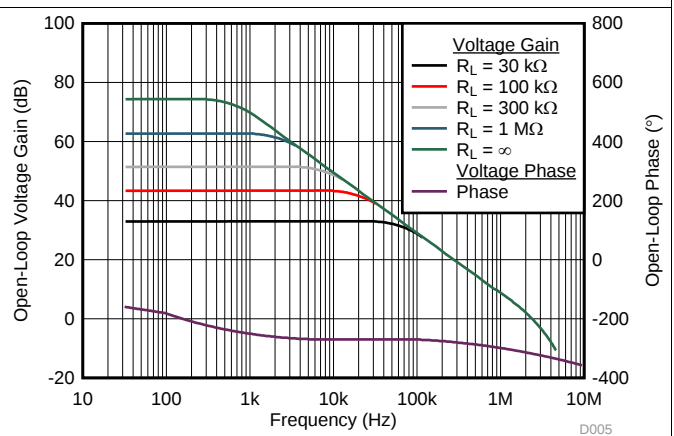


Figure 4. Error Amplifier Voltage Gain and Phase vs Frequency

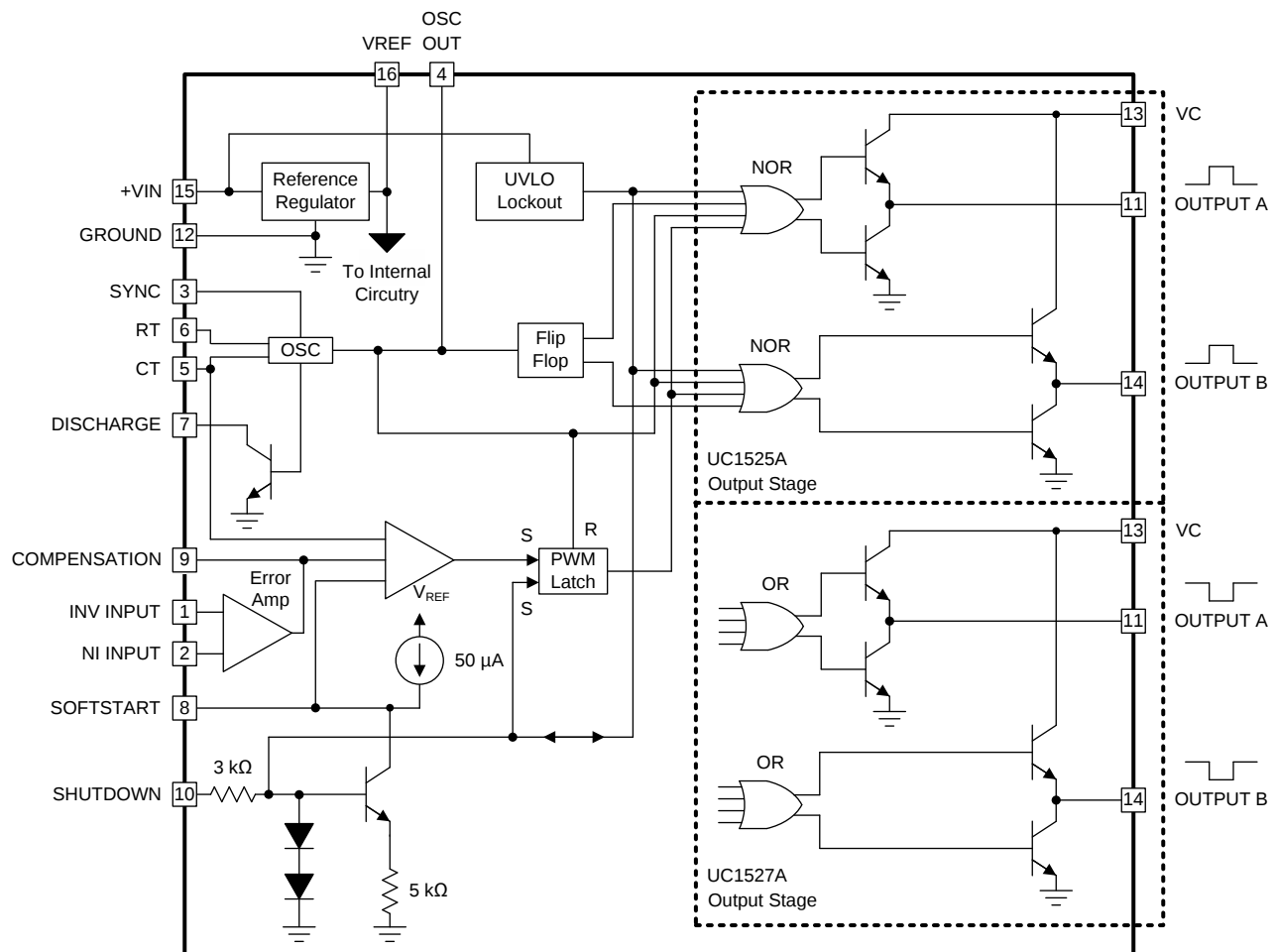
7 Detailed Description

7.1 Overview

The UCx52xA series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip 5.1-V reference is trimmed to 1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between CT and the discharge terminals provides a wide range of dead-time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands.

These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for subnormal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The UC1525A output stage features NOR logic, giving a LOW output for an OFF state. The UC1527A uses OR logic, which results in a HIGH output level when OFF.

7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 Adjustable Dead-Time Control

A single resistor between CT and the discharge terminals provides a wide range of dead-time adjustment.

7.3.2 Soft Start

Soft start is achieved by connecting the soft-start pin to ground through a capacitor, charged by the 50- μ A current source. See [Functional Block Diagram](#).

7.3.3 Input Undervoltage Lockout With Hysteresis

The undervoltage lockout keeps the outputs off and the soft-start capacitor discharged for subnormal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitter-free operation.

7.3.4 Shutdown and Pulse-by-Pulse Current Limiting

See [Shutdown Options \(See Functional Block Diagram\)](#).

7.4 Device Functional Modes

This device has no functional modes.

7.4.1 Shutdown Options (See [Functional Block Diagram](#))

Since both the compensation and soft-start terminals have current source pullups, either can readily accept a pull-down signal which only has to sink a maximum of 100 A to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of the shutdown pin which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on the shutdown pin performs two functions; the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150-A current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding the shutdown pin high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turnon upon release.

The shutdown pin should not be left floating as noise pickup could conceivably interrupt normal operation. All transitions of the voltage on the shutdown pin should be within the time frame of one clock cycle and not repeated at a frequency higher than 10 clock cycles.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UC1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The UC1525A output stage features NOR logic, giving a LOW output for an OFF state. The UC1527A utilizes OR logic which results in a HIGH output level when OFF.

8.2 Typical Application

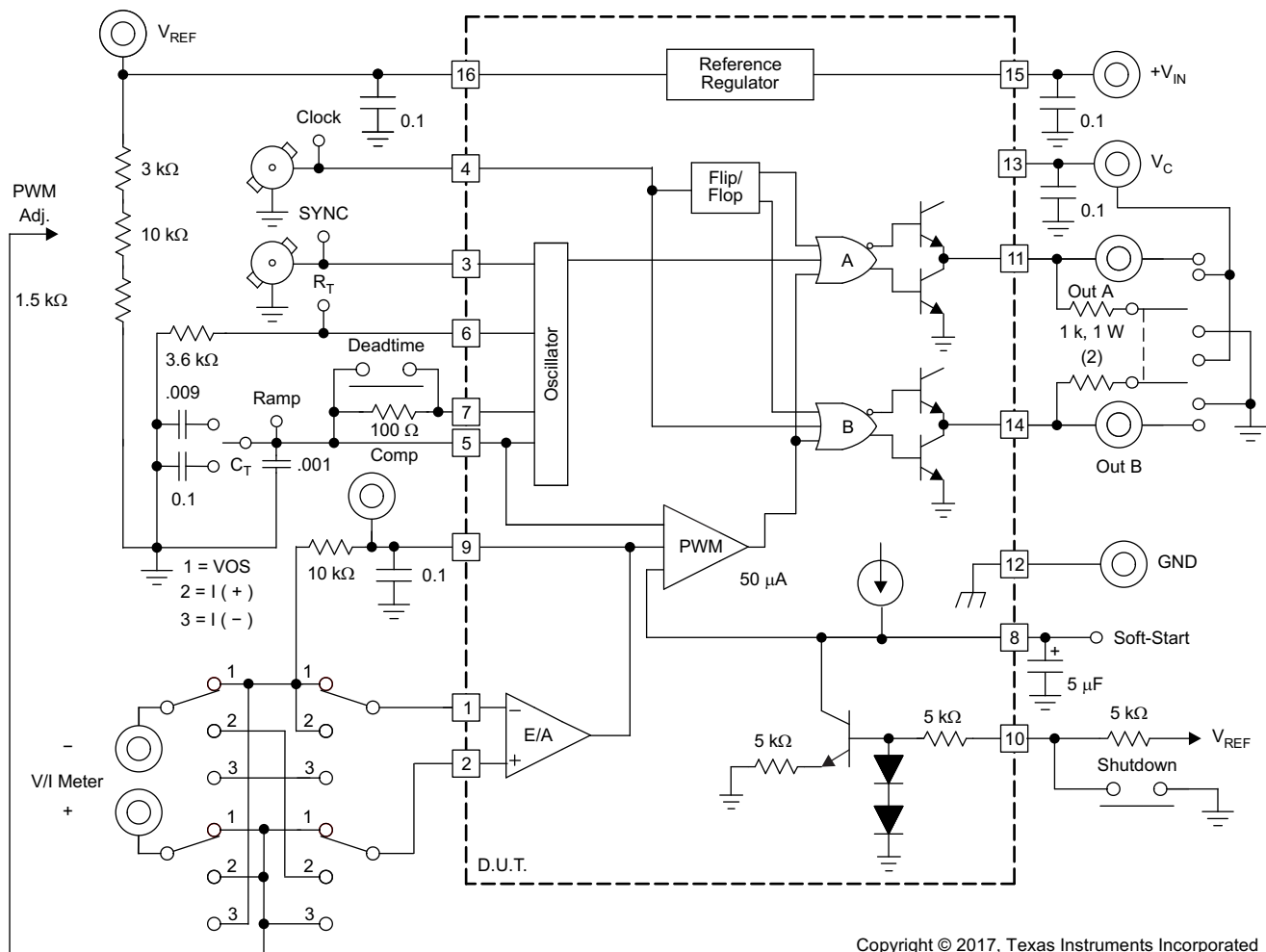


Figure 5. Lab Test Fixture

Typical Application (continued)

8.2.1 Theory of Operation

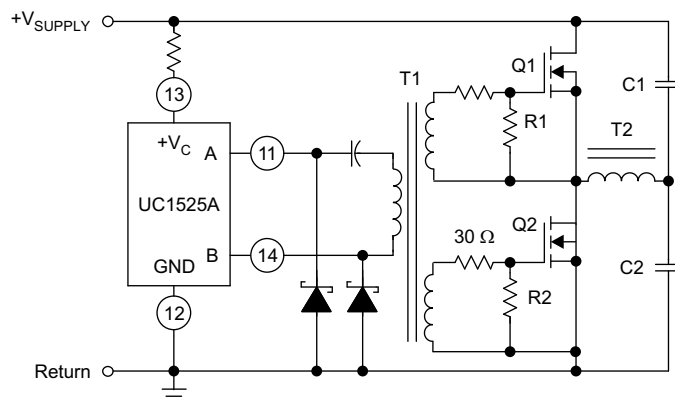


Figure 6. Low Power Transformers

Low power transformers can be driven by the UC1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

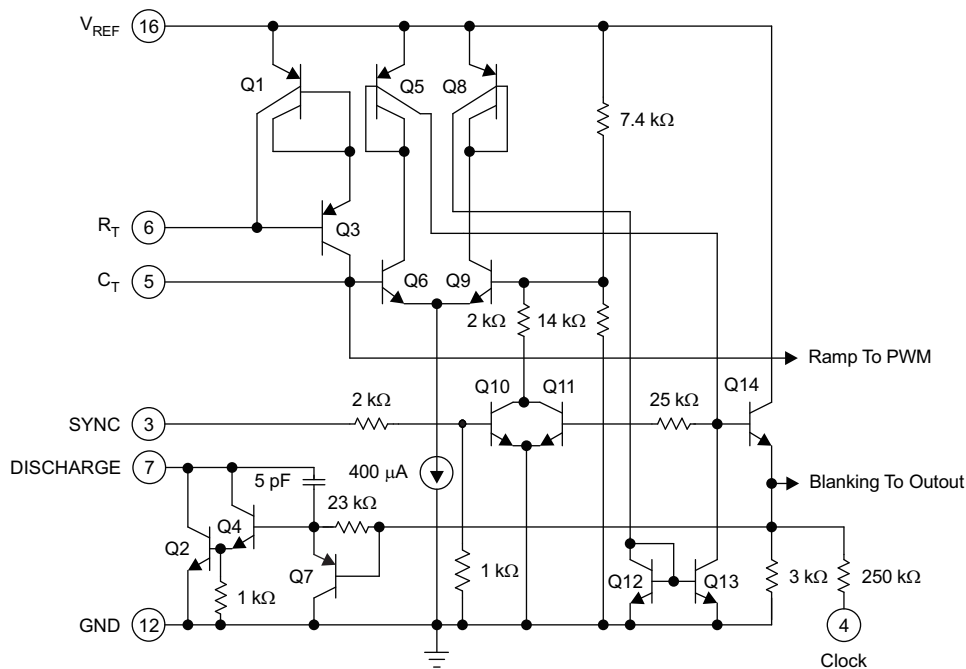


Figure 7. UC1525A Oscillator Schematic

Figure 8. UC1525A Error Amplifier

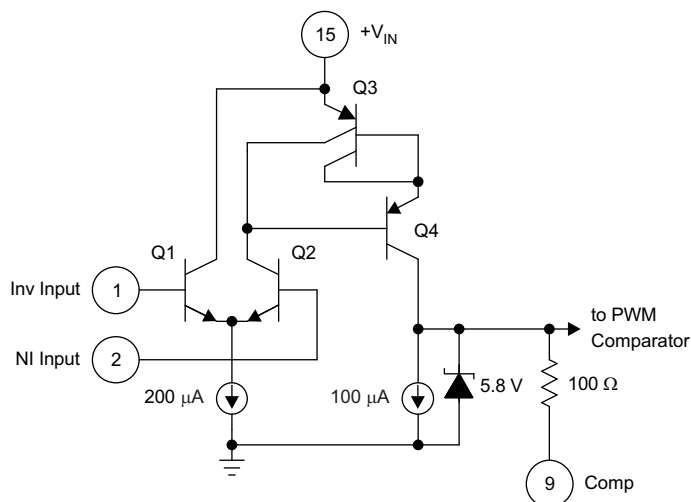


Figure 9. UC1525A Output Circuit (1/2 circuit shown)

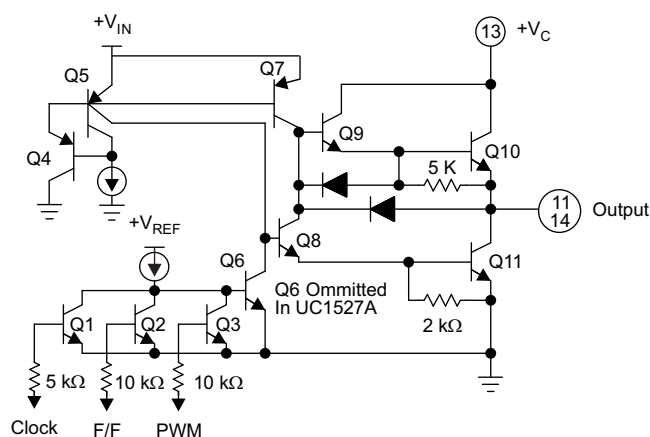
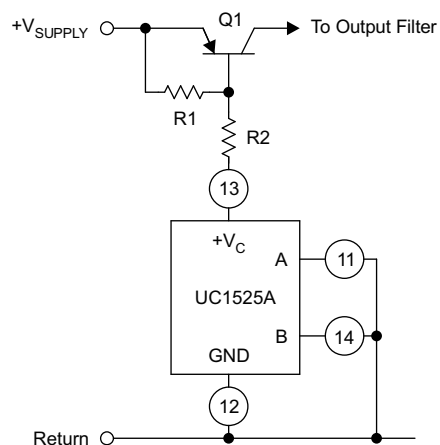


Figure 10. Grounded Driver Outputs For Single-Ended Supplies



Typical Application (continued)

For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

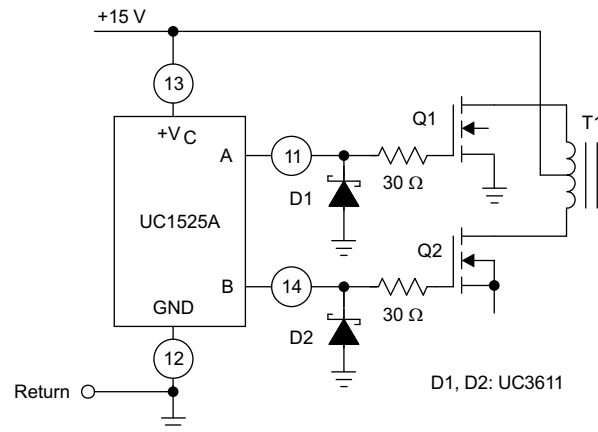


Figure 11. Output Drivers With Low Source Impedance

The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

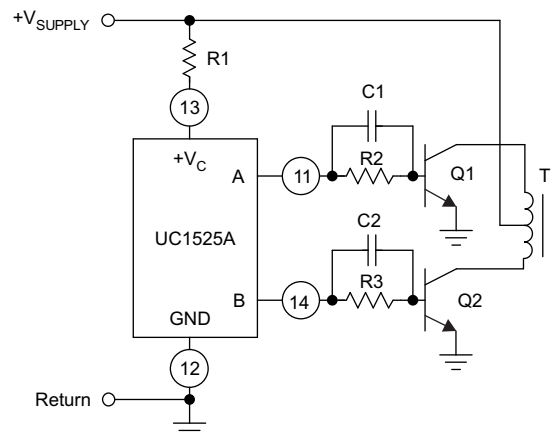


Figure 12. Conventional Push-Pull Bipolar Design

In conventional push-pull bipolar designs, forward base drive is controlled by R1–R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

8.2.2 Design Requirements

This example illustrates the design process and component selection for a push-pull DC-DC converter utilizing the UC1525A. The converter regulates a 30-V input to a 5-V output with 10-A maximum load.

Table 1. Design Parameters

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	25	30	35	V
V_{OUT}	Output voltage		5		V
i_{OUT}	Output current	1		10	A
f_O	Oscillator frequency		100		kHz
f_S	Switching frequency		50		kHz

8.2.3 Detailed Design Procedure

8.2.3.1 Timing Resistor and Capacitor Selection

Generally, higher switching frequency gives smaller size but have higher switching loss. Operation at 100 kHz was selected in this example as a reasonable compromise between size and efficiency. The value of $R_T = 10\text{ k}\Omega$, $C_T = 1.37\text{ nF}$ and $R_D = 100\text{ }\Omega$ were chosen for 100-kHz oscillator frequency based on equation:

$$f = \frac{1}{C_T(0.7 R_T + 3 R_D)} \quad (1)$$

8.2.3.2 Turns Ratio Selection

The maximum primary-to-secondary turns ratio N_{MAX} can be determined by the target output voltage, minimum input voltage, and the estimated maximum duty cycle. $D_{LIM} = 0.35$ was selected for this example. N_{MAX} can be calculated using Equation 1.

$$N_{MAX} = \frac{2 \times D_{LIM} \times V_{IN(min)}}{V_{OUT} + V_F} = \frac{2 \times 0.35 \times 25\text{ V}}{5\text{ V} + 0.3\text{ V}} = 3.3 \quad (2)$$

Rounding N_{MAX} down to the next lowest integer results in a turns ratio of $N = 3$.

8.2.3.3 Inductor Selection

The maximum inductor ripple current occurs at the maximum input voltage. Typically, 20% to 40% of the full load current ripple is a good compromise between core loss and copper loss of the inductor. Higher ripple current allows for a smaller inductor size, but places more burden on the output capacitor to smooth the ripple voltage on the output. In this example, a ripple current of 25% of 10 A was chosen. The inductor value can be calculated as:

$$L_O = \frac{V_{OUT} + V_F}{\Delta I_L \times f_{SW}} \times \left(\frac{1}{2} - \frac{N \times (V_{OUT} + V_F)}{2 \times V_{IN(max)}} \right) = 11.57\text{ }\mu\text{H} \quad (3)$$

8.2.3.4 Rectification Diode Selection

A rectification diode should always possess low-forward voltage drop. When used in high-frequency switching applications, the diode must also possess a short recovery time. Schottky diodes meet both requirements and are therefore strongly recommended in push-pull converter designs.

8.2.3.5 VC Capacitor Selection

The primary purpose of the VC capacitor is to supply the peak transient currents of the drivers as well as provide stability for the VC regulator. These peak currents can be several amperes. The recommended value of VC capacitor should be no smaller than $0.1\text{ }\mu\text{F}$, and should be a good quality, low ESR, ceramic capacitor. VC capacitor should be placed as close as possible to the VC pin to minimize potentially damaging voltage transients caused by trace inductance.

8.2.3.6 Output Capacitor Selection

The output capacitors smooth the output voltage ripple caused by inductor ripple current and provide a source of charge during load transient conditions.

8.2.3.7 Input Capacitor Selection

The input supply voltage typically has high source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. The input capacitor should be selected for RMS current rating and minimum ripple voltage.

8.2.4 Application Curves

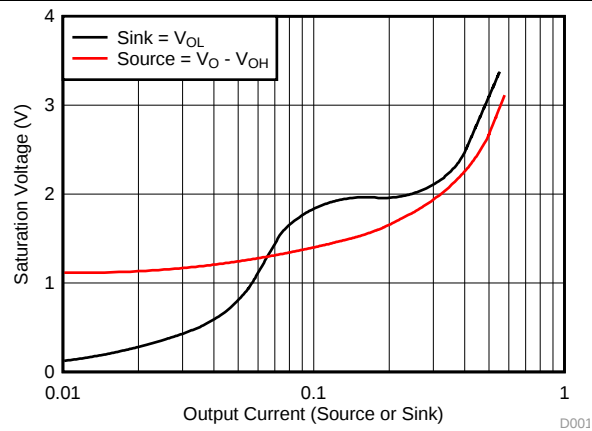


Figure 13. UC1525A Output Saturation Characteristics

9 Power Supply Recommendations

The voltage range for V_{IN} is 8 V to 35 V.

The voltage range for V_C is 4.5 V to 35 V. Choose a voltage level which is suitable for the power switch, for example, 12 V for MOSFET.

10 Layout

10.1 Layout Guidelines

High-speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1525A follow these rules:

- Use a ground plane
- Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1-A Schottky diode at the output pin will serve this purpose.
- Bypass V_{IN} , V_C , and V_{REF} . Use 0.1- μ F monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane.
- Treat the timing capacitor, C_T , like a bypass capacitor.

10.2 Layout Example

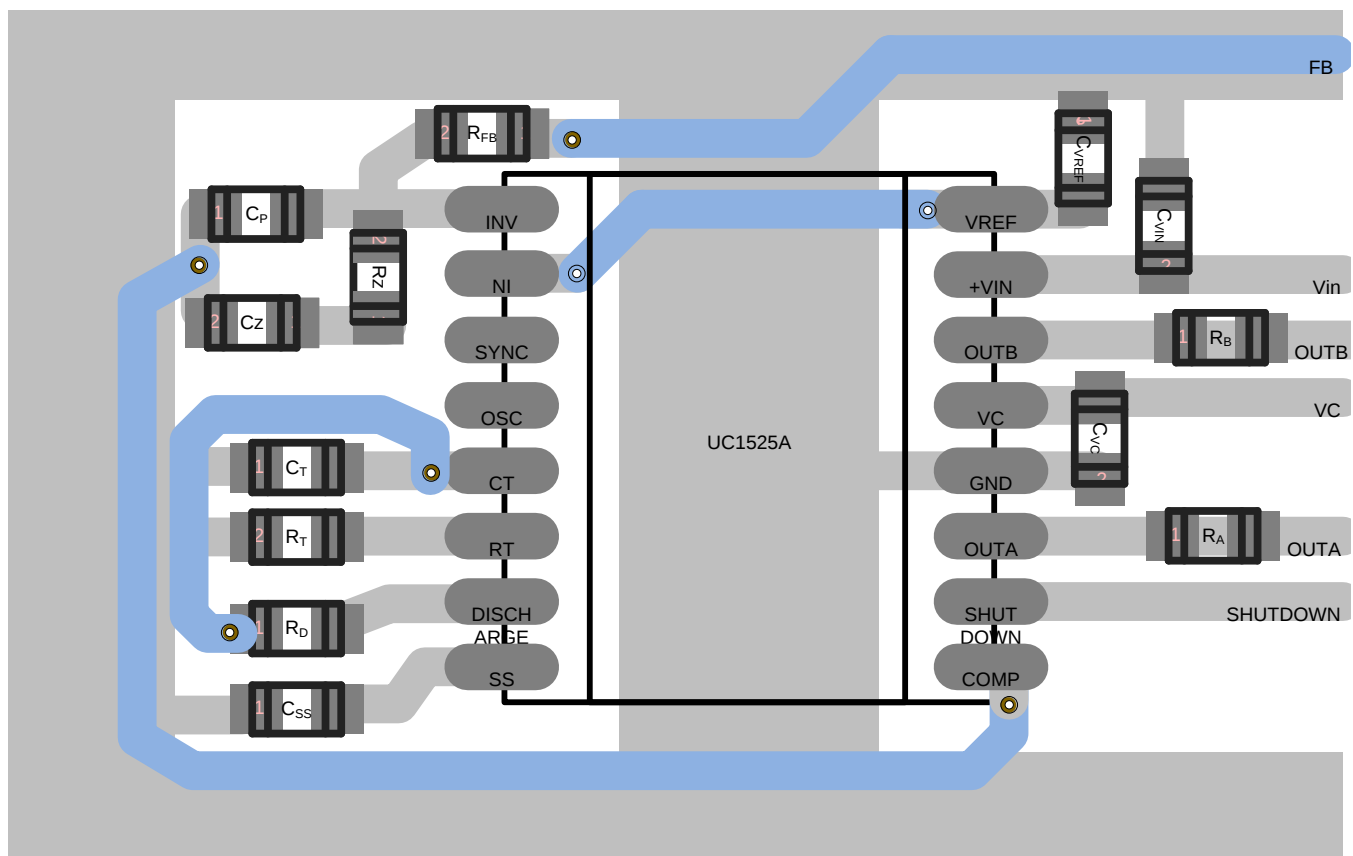


Figure 14. UC1525A Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

[Switching Power Supply Topology Voltage Mode vs Current Mode](#) (SLUA119)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UC1525A	Click here	Click here	Click here	Click here	Click here
UC1527A	Click here	Click here	Click here	Click here	Click here
UC2525A	Click here	Click here	Click here	Click here	Click here
UC2527A	Click here	Click here	Click here	Click here	Click here
UC3525A	Click here	Click here	Click here	Click here	Click here
UC3527A	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-89511032A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 89511032A UC1525AL/ 883B	Samples
5962-8951103EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8951103EA UC1525AJ/883B	Samples
5962-8951104EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8951104EA UC1527AJ/883B	Samples
UC1525AJ	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	UC1525AJ	Samples
UC1525AJ883B	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8951103EA UC1525AJ/883B	Samples
UC1525AL	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	UC1525AL	Samples
UC1525AL883B	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 89511032A UC1525AL/ 883B	Samples
UC1527AJ	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	UC1527AJ	Samples
UC1527AJ883B	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8951104EA UC1527AJ/883B	Samples
UC2525ADW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-25 to 85	UC2525ADW	
UC2525ADWTR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2525ADW	Samples
UC2525AJ	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-25 to 85	UC2525AJ	Samples
UC2525AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	UC2525AN	Samples
UC2525ANG4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	UC2525AN	Samples
UC2525BDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2525BDW	Samples
UC2525BN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	UC2525BN	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2527AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	UC2527AN	Samples
UC3525ADW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525ADW	Samples
UC3525ADWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525ADW	Samples
UC3525ADWTR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525ADW	Samples
UC3525ADWTRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525ADW	Samples
UC3525AJ	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	0 to 70	UC3525AJ	Samples
UC3525AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3525AN	Samples
UC3525ANG4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3525AN	Samples
UC3527AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3527AN	Samples
UC3527ANG4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3527AN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

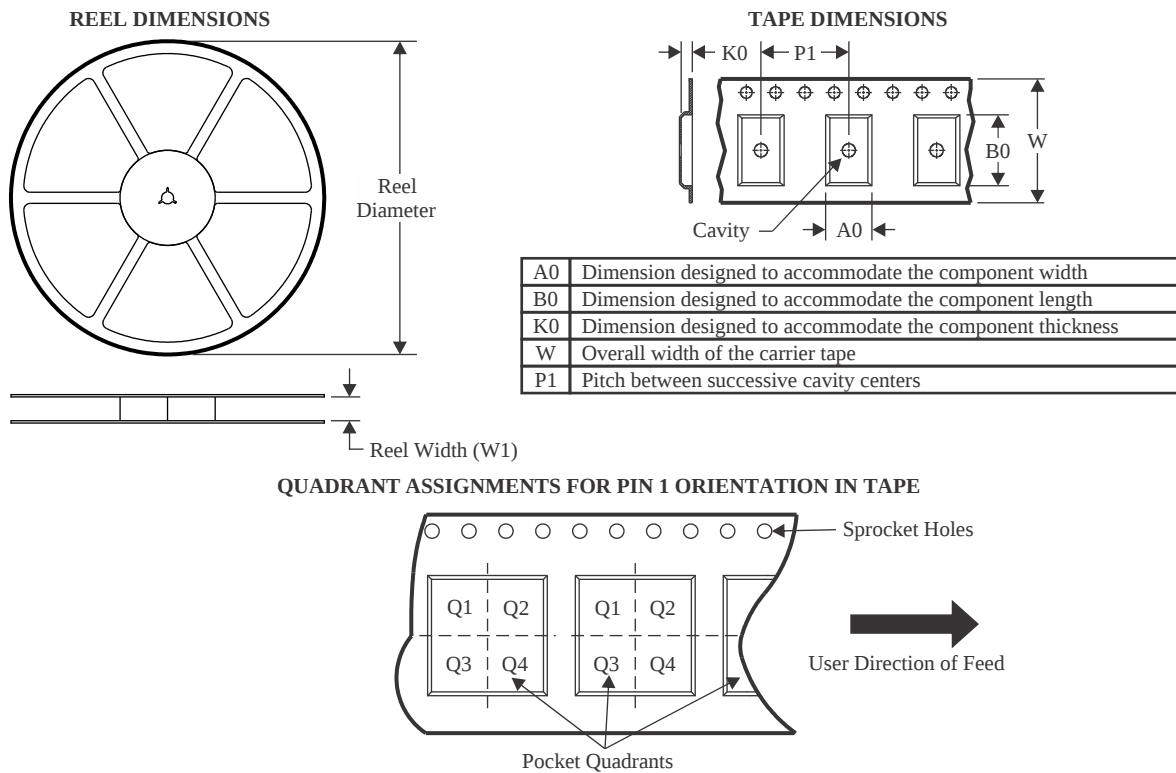
OTHER QUALIFIED VERSIONS OF UC1525A, UC1527A, UC2525A, UC2525AM, UC3525A, UC3525AM, UC3527A :

- Catalog : [UC3525A](#), [UC3527A](#), [UC2525A](#), [UC3525AM](#), [UC3525A](#)
- Military : [UC2525AM](#), [UC1525A](#), [UC1525A](#), [UC1527A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

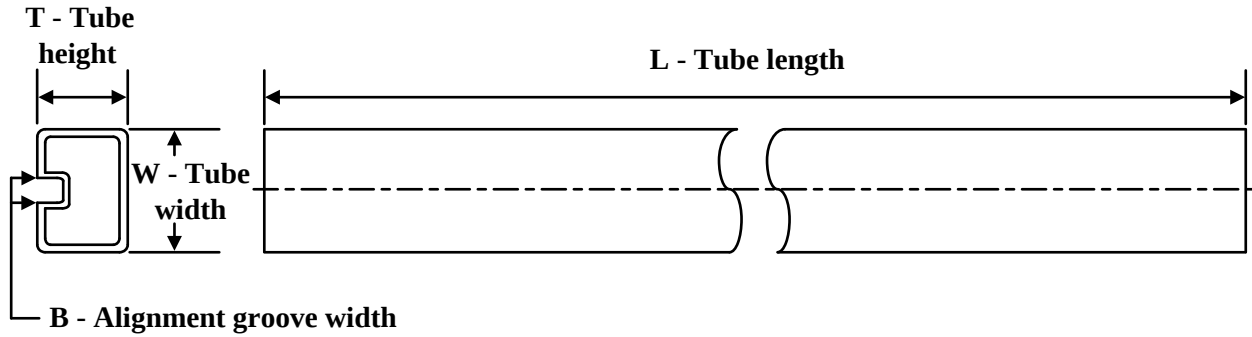
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2525ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3525ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2525ADWTR	SOIC	DW	16	2000	356.0	356.0	35.0
UC3525ADWTR	SOIC	DW	16	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-89511032A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1525AL	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1525AL883B	FK	LCCC	20	55	506.98	12.06	2030	NA
UC2525AN	N	PDIP	16	25	506	13.97	11230	4.32
UC2525ANG4	N	PDIP	16	25	506	13.97	11230	4.32
UC2525BDW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2525BN	N	PDIP	16	25	506	13.97	11230	4.32
UC2527AN	N	PDIP	16	25	506	13.97	11230	4.32
UC3525ADW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3525ADWG4	DW	SOIC	16	40	507	12.83	5080	6.6
UC3525AN	N	PDIP	16	25	506	13.97	11230	4.32
UC3525ANG4	N	PDIP	16	25	506	13.97	11230	4.32
UC3527AN	N	PDIP	16	25	506	13.97	11230	4.32
UC3527ANG4	N	PDIP	16	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

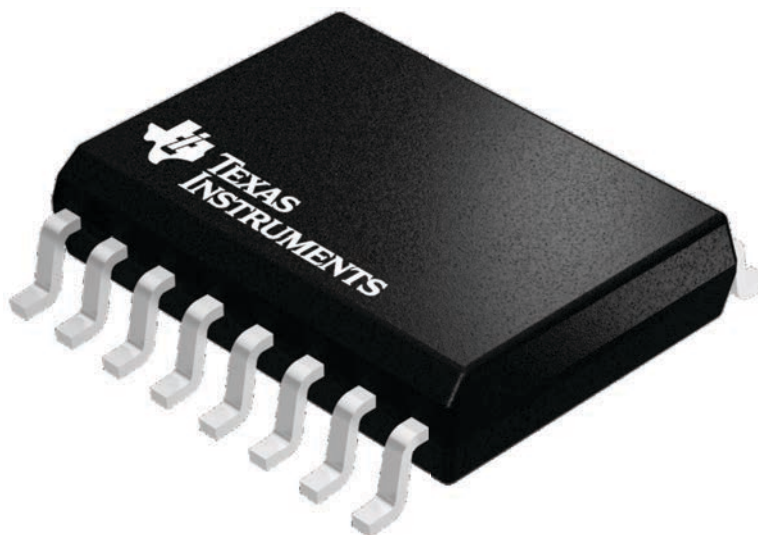
DW 16

SOIC - 2.65 mm max height

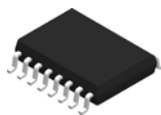
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

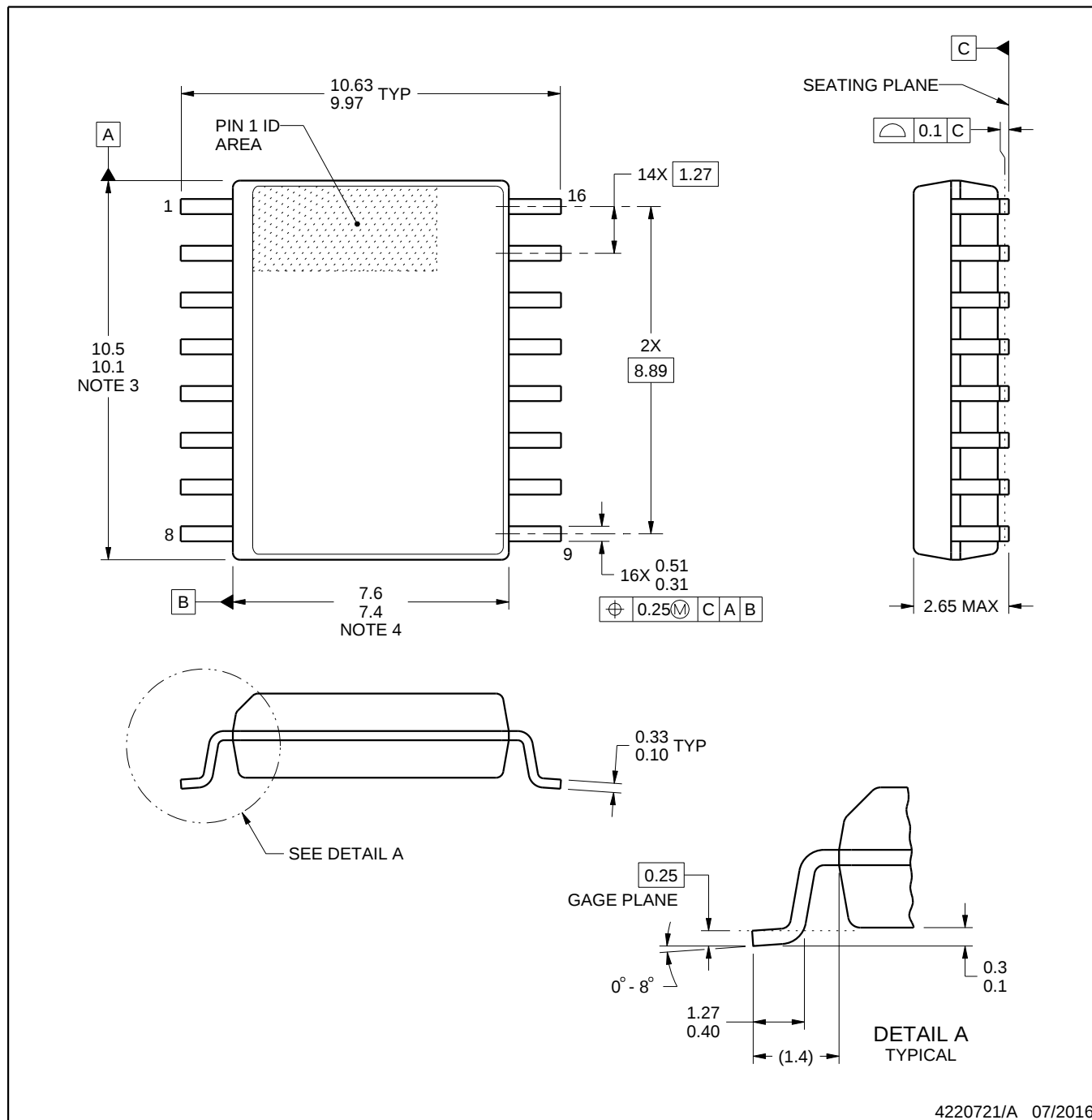


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

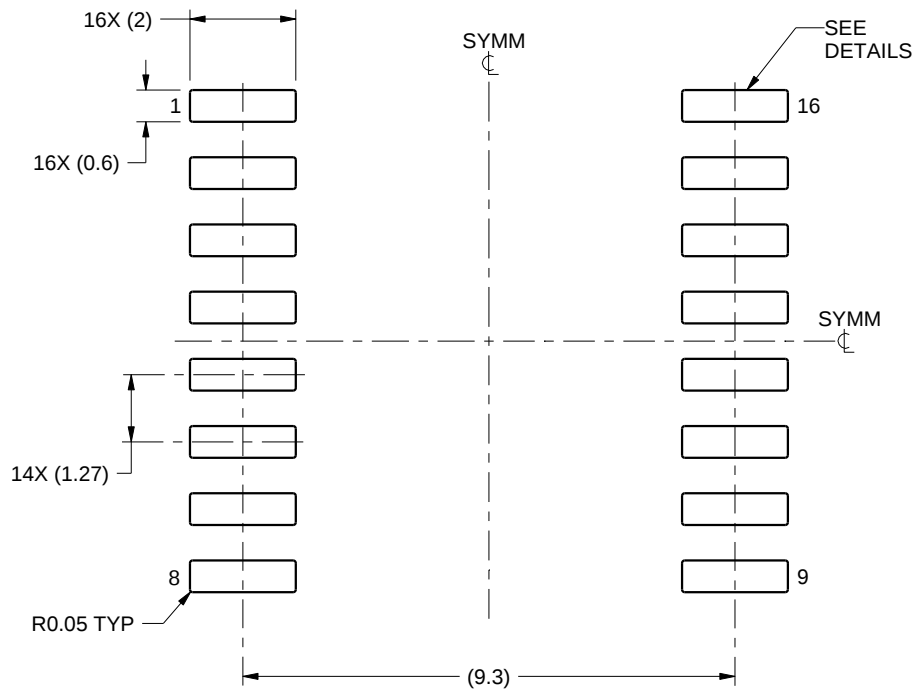
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

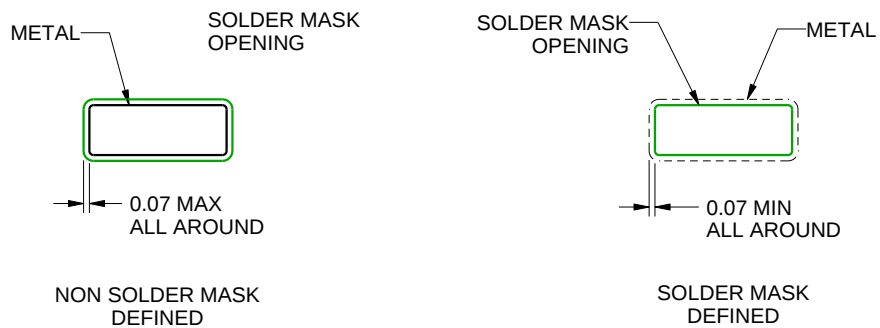
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

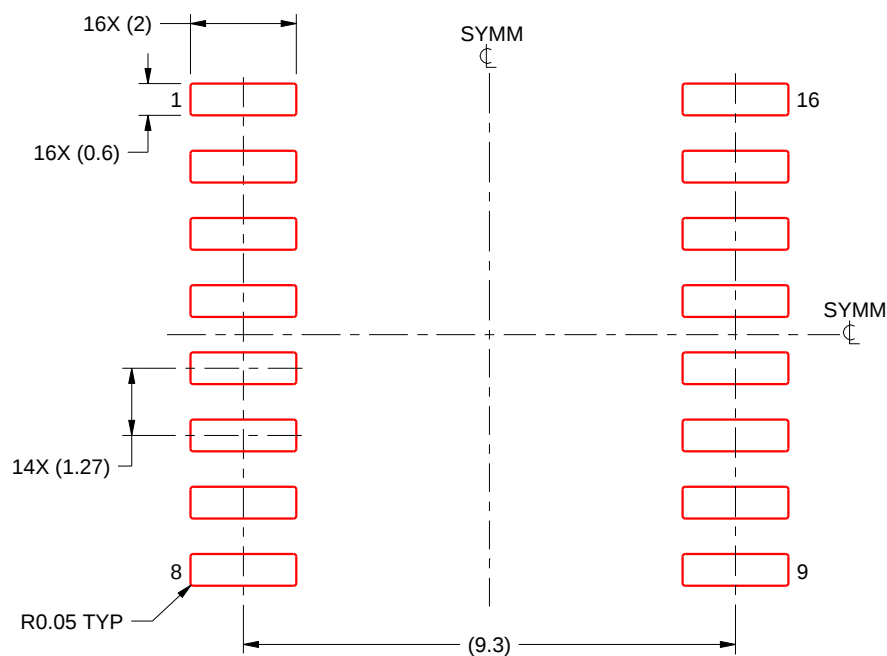
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

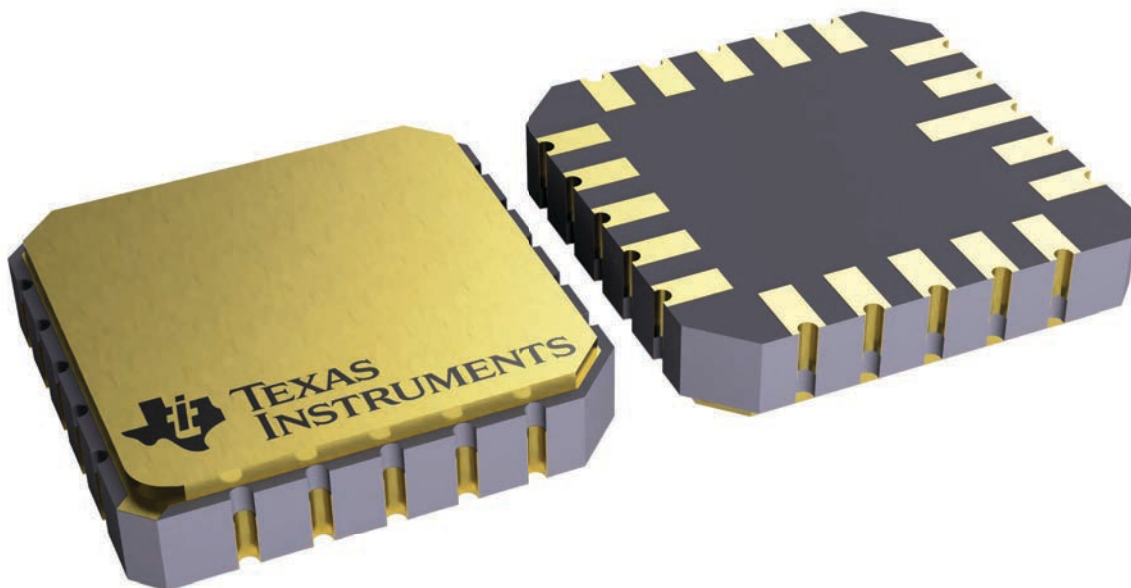
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

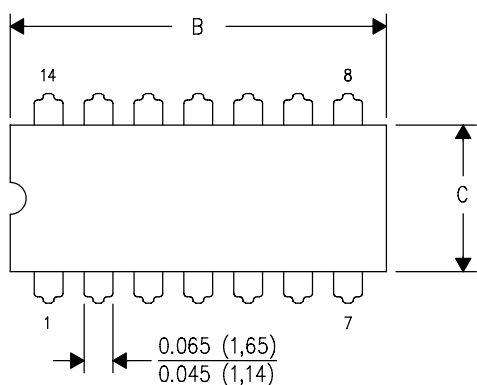


4229370VA\

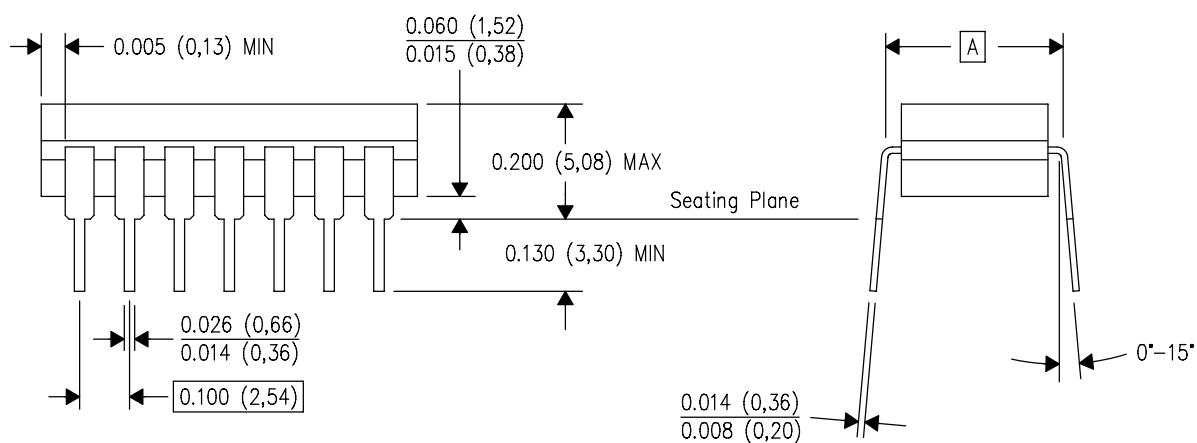
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



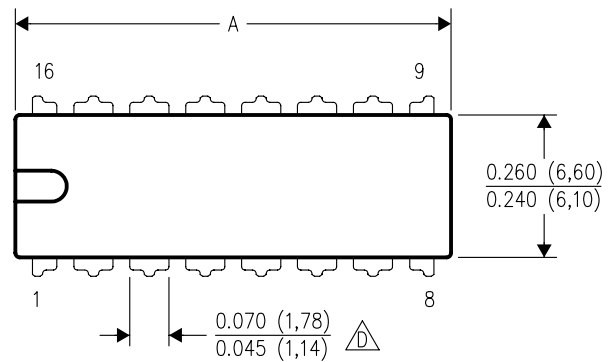
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

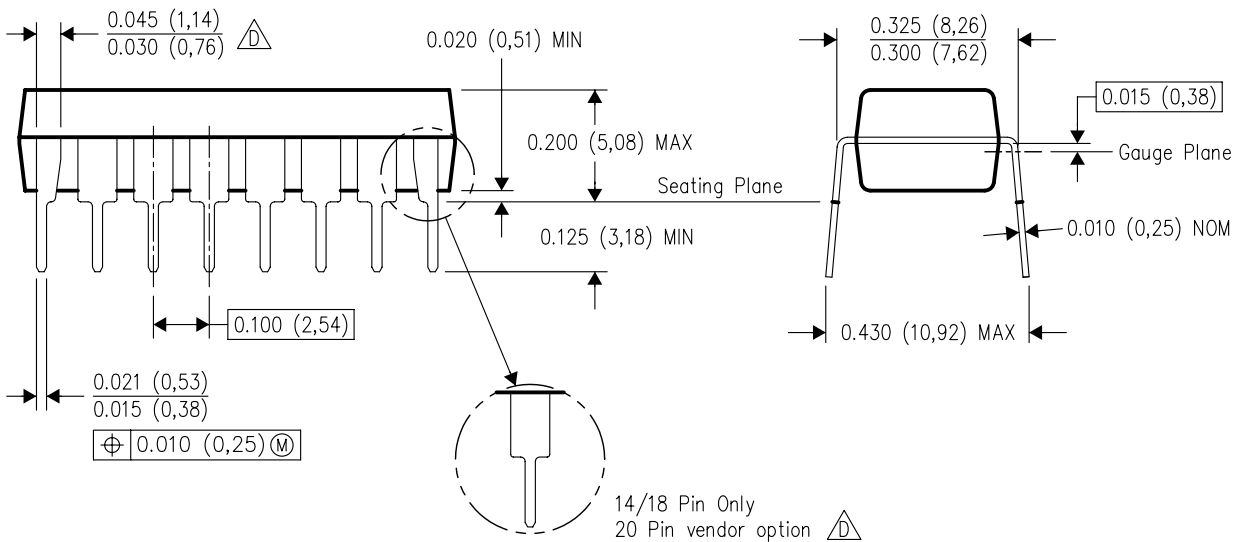
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated