



AOT22N50/AOTF22N50

500V, 22A N-Channel MOSFET

General Description

The AOT22N50 & AOTF22N50 have been fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low $R_{DS(on)}$, C_{iss} and C_{rss} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

For Halogen Free add "L" suffix to part number:
AOT22N50L & AOTF22N50L

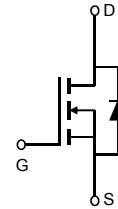
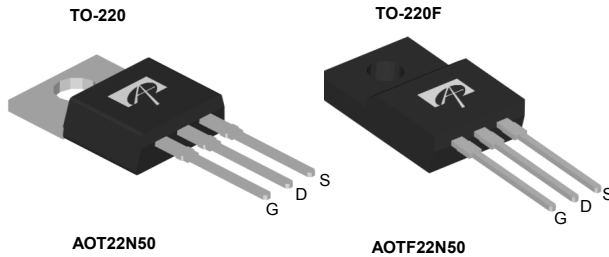
Product Summary

V_{DS}	600V@150°C
I_D (at $V_{GS}=10V$)	22A
$R_{DS(on)}$ (at $V_{GS}=10V$)	< 0.26Ω

100% UIS Tested
100% R_g Tested



Top View



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOT22N50L	TO220 Green	Tube	1000
AOTF22N50	TO-220F Pb Free	Tube	1000
AOTF22N50L	TO-220F Green	Tube	1000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	AOT22N50	AOTF22N50	AOTF22N50L	Units
Drain-Source Voltage	V_{DS}	500			V
Gate-Source Voltage	V_{GS}	± 30			V
Continuous Drain Current	$T_C=25^\circ\text{C}$	22	22*	22*	A
	$T_C=100^\circ\text{C}$	15	15*	15*	
Pulsed Drain Current ^C	I_{DM}	88			A
Avalanche Current ^C	I_{AR}	7			A
Repetitive avalanche energy ^C	E_{AR}	735			mJ
Single pulsed avalanche energy ^G	E_{AS}	1470			mJ
Peak diode recovery dv/dt	dv/dt	5			V/ns
Power Dissipation ^B	$T_C=25^\circ\text{C}$	417	50	39	W
	Derate above 25°C	3.3	0.4	0.3	W/°C
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150			°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300			°C

Thermal Characteristics

Parameter	Symbol	AOT22N50	AOTF22N50	AOTF22N50L	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	65	65	65	°C/W
Maximum Case-to-sink ^A	$R_{\theta CS}$	0.5	--	--	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	0.3	2.5	3.2	°C/W

* Drain current limited by maximum junction temperature.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	500			V
		I _D =250μA, V _{GS} =0V, T _J =150°C		600		
BV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D =250μA, V _{GS} =0V		0.57		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =500V, V _{GS} =0V			1	μA
		V _{DS} =400V, T _J =125°C			10	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V I _D =250μA	3.4	4	4.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =11A		0.21	0.26	Ω
g _{FS}	Forward Transconductance	V _{DS} =40V, I _D =11A		25		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				22	A
I _{SM}	Maximum Body-Diode Pulsed Current				88	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =25V, f=1MHz	2465	3086	3710	pF
C _{oss}	Output Capacitance		200	290	380	pF
C _{rss}	Reverse Transfer Capacitance		14	24	35	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.7	1.4	2.1	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =400V, I _D =22A	55	69	83	nC
Q _{gs}	Gate Source Charge		17	22	27	nC
Q _{gd}	Gate Drain Charge		12	24	36	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =250V, I _D =22A, R _G =25Ω		60		ns
t _r	Turn-On Rise Time			122		ns
t _{D(off)}	Turn-Off DelayTime			124		ns
t _f	Turn-Off Fall Time			77		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =22A, dI/dt=100A/μs, V _{DS} =100V	415	524	630	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =22A, dI/dt=100A/μs, V _{DS} =100V	7.5	9.6	12	μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25° C.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. L=60mH, I_{AS}=7A, V_{DD}=150V, R_G=25Ω, Starting T_J=25° C

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

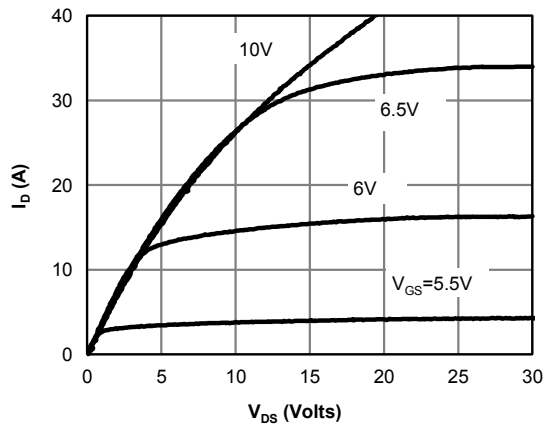


Fig 1: On-Region Characteristics

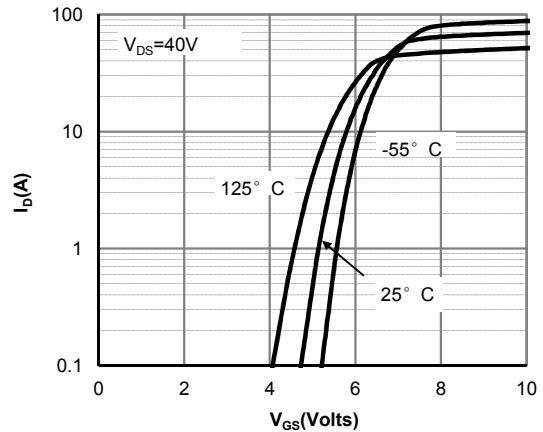


Figure 2: Transfer Characteristics

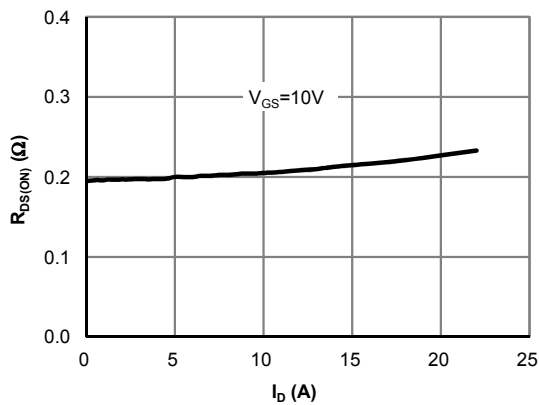


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

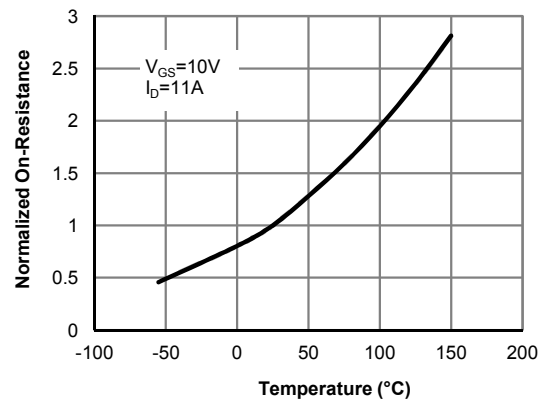


Figure 4: On-Resistance vs. Junction Temperature

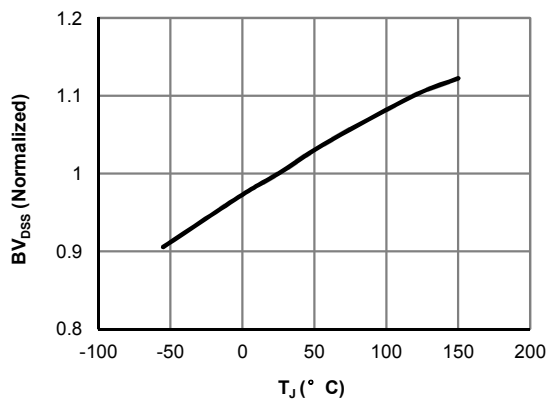


Figure 5: Break Down vs. Junction Temperature

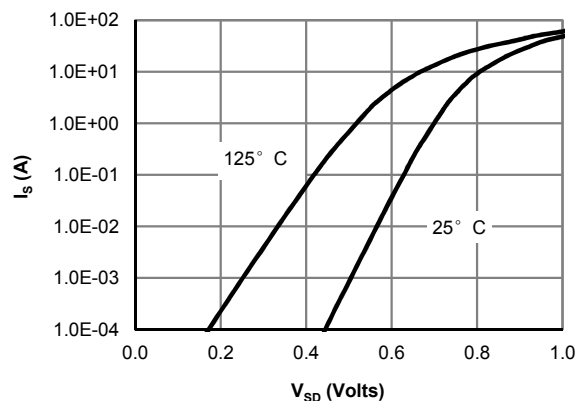


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

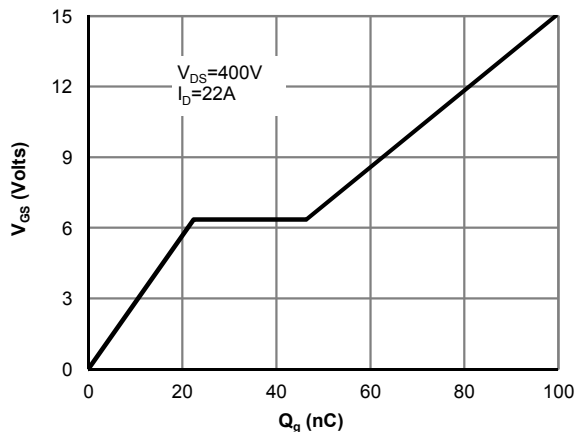


Figure 7: Gate-Charge Characteristics

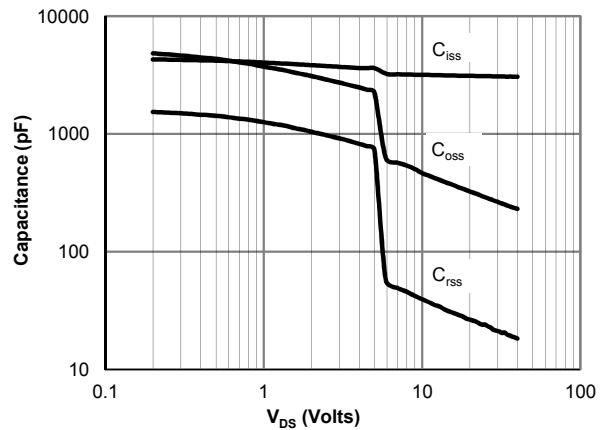


Figure 8: Capacitance Characteristics

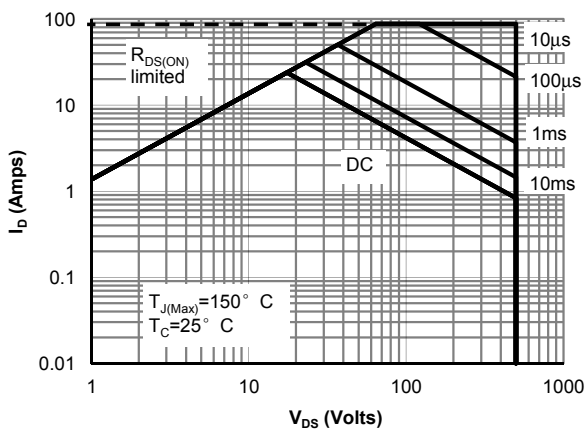


Figure 9: Maximum Forward Biased Safe Operating Area for AOT22N50 (Note F)

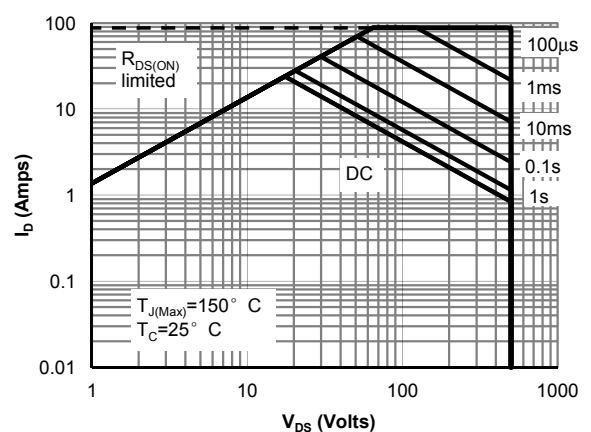


Figure 10: Maximum Forward Biased Safe Operating Area for AOTF22N50 (Note F)

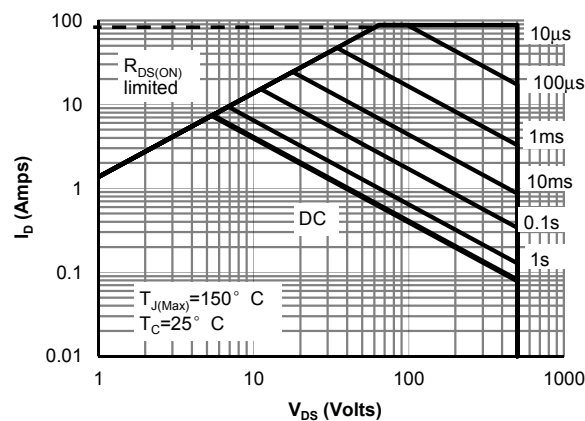


Figure 12: Maximum Forward Biased Safe Operating Area for AOTF22N50L (Note F)

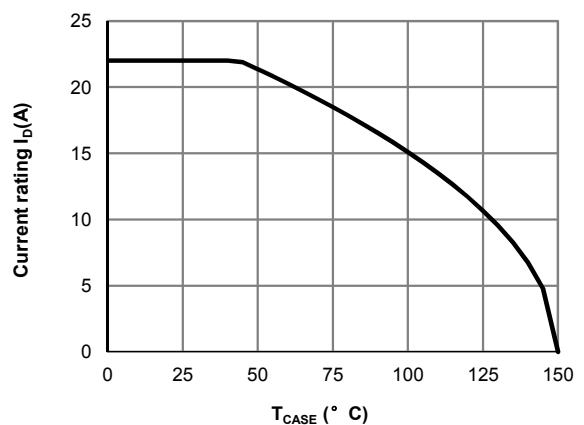


Figure 11: Current De-rating (Note B)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

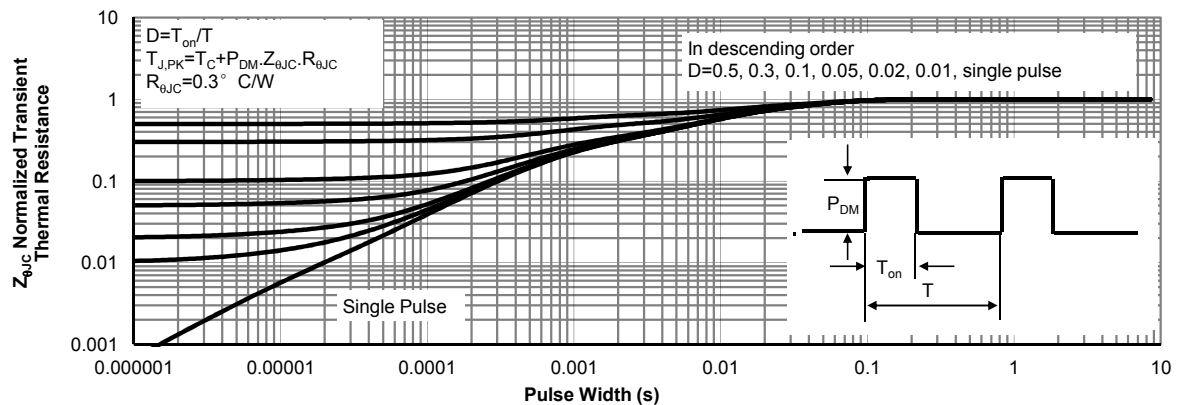


Figure 13: Normalized Maximum Transient Thermal Impedance for AOT22N50 (Note F)

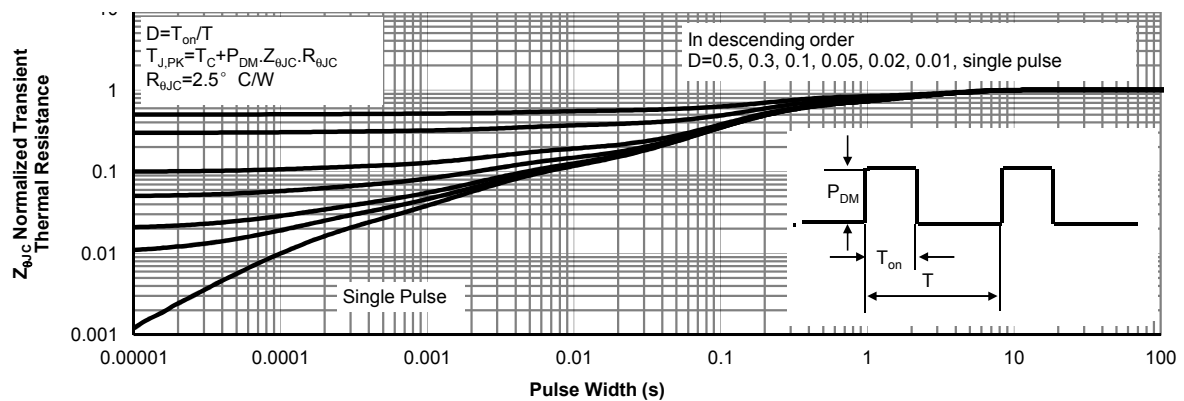


Figure 14: Normalized Maximum Transient Thermal Impedance for AOTF22N50 (Note F)

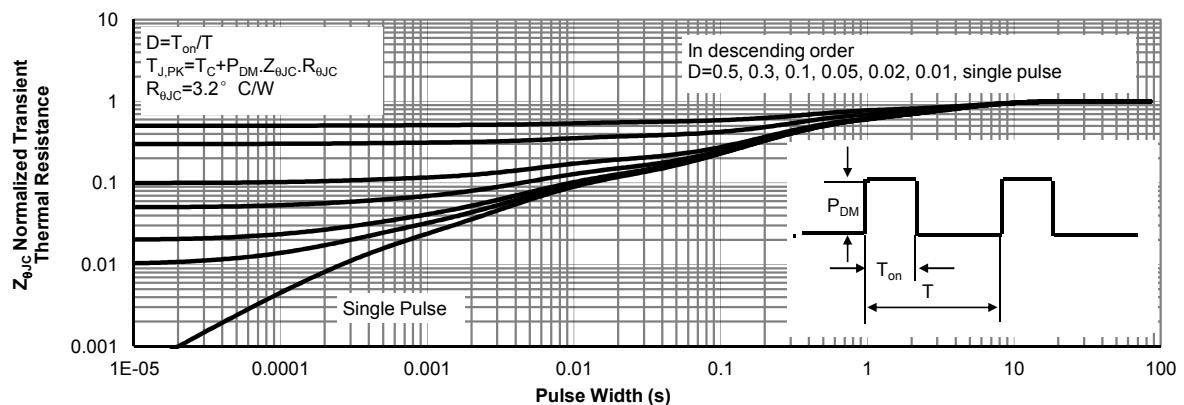
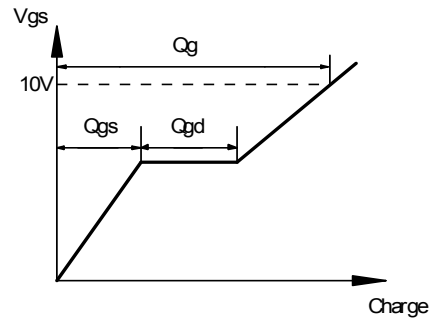
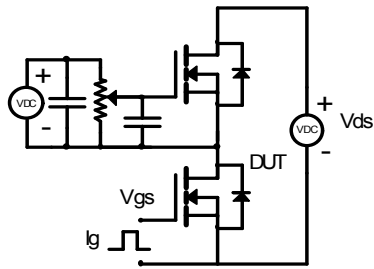
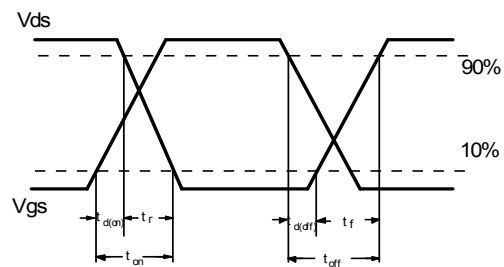
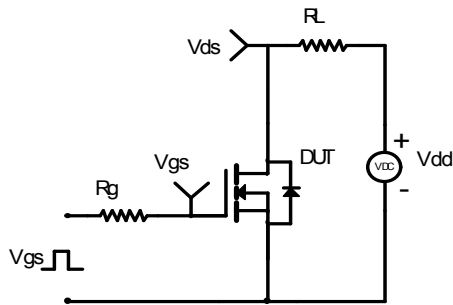


Figure 15: Normalized Maximum Transient Thermal Impedance for AOTF22N50L (Note F)

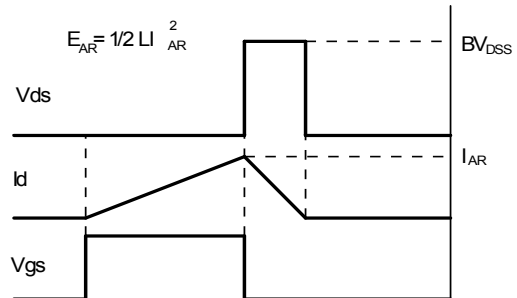
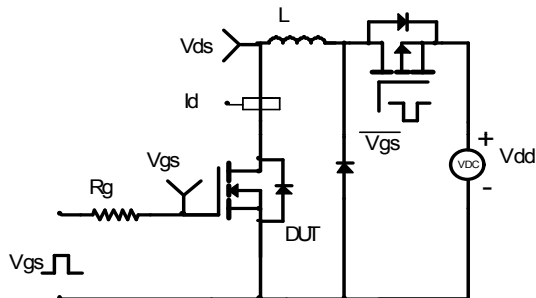
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

