IRS2461S

400V Class D Audio Amplifier Controller

Features

- Single channel integrated analog input Class D audio amplifier driver
- 400V high voltage gate driver stage
- Differential or single-ended input
- Versatile protection control enabling latched, non-latched, or host controlled shutdown function
- Programmable over current protection
- Programmable dead-time generation
- External thermal sensor input
- Click noise reduction
- Under voltage protection
- High noise immunity

Product summary

Product feature	Key specification
Topology	Half-Bridge/Full-Bridge
$V_{OFFSET\ (max)}$	+/- 200 V
I_{O+} & I_{O-} (typical)	0.5 A & 0.6 A
Selectable deadtime	165/225/280/340 ns
DC offset	<18 mV
OC protection delay	500 ns (max)
Shutdown propagation delay	250 ns (max)
Error amplifier open loop gain	>60 dB

Potential applications

- High voltage high power Class D audio amplifier
- High voltage high power PWM amplifier

Product validation

Qualified for industrial applications according to the relevant JEDEC47/20/22

Ordering information

Base Part Number	Package Type	Standard Pack Form and Quantity	
IRS2461S	20 Lead SOICWB	Tape and Reel	1000

Description

The IRS2461S integrates high voltage, high performance Class D audio amplifier drivers with PWM modulator and protections. In conjunction with external MOSFET, the IRS2461S forms a single channel Class D audio amplifier. The IRS2461S is designed with floating analog inputs and protection control interface pins convenient for half bridge applications. High and low side MOSFETs are protected from over current conditions by a programmable over current protection. Essential elements of PWM modulator section allow flexible system design. The IRS2461S is a lead-free, ROHS compliant.

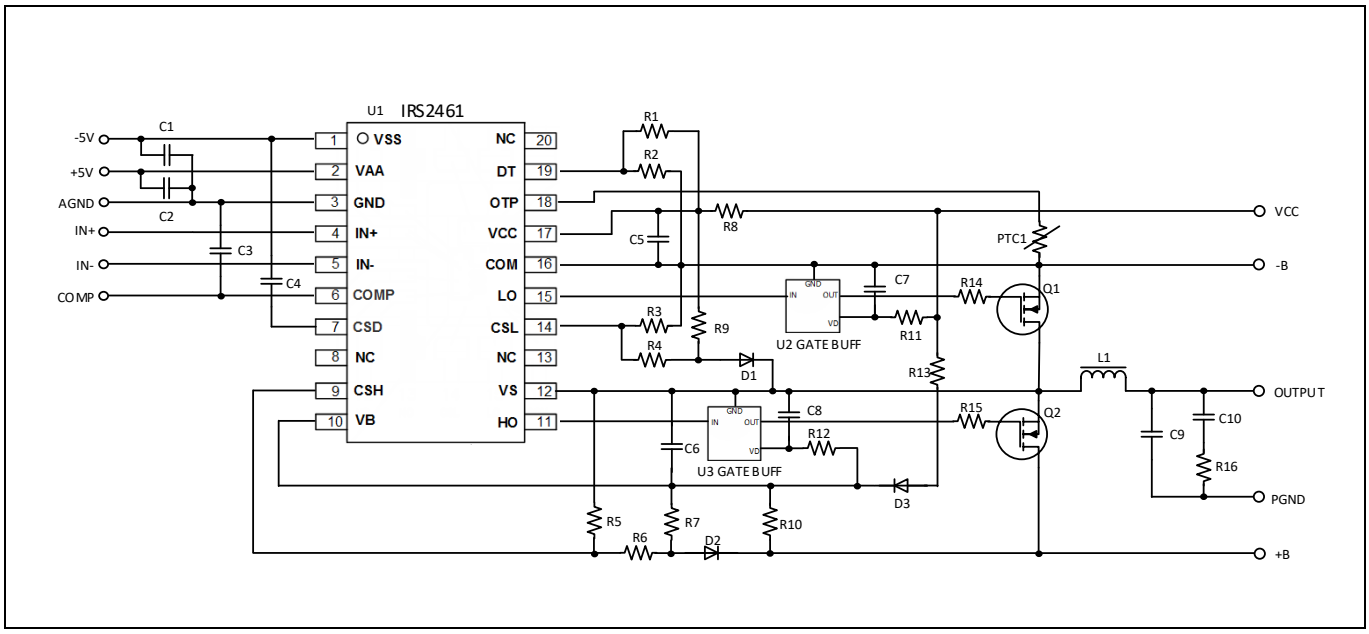

Figure 1 Typical application

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1 Pin configuration and functionality

The pin configuration is shown in Figure 2 and the functions are described in Table A.

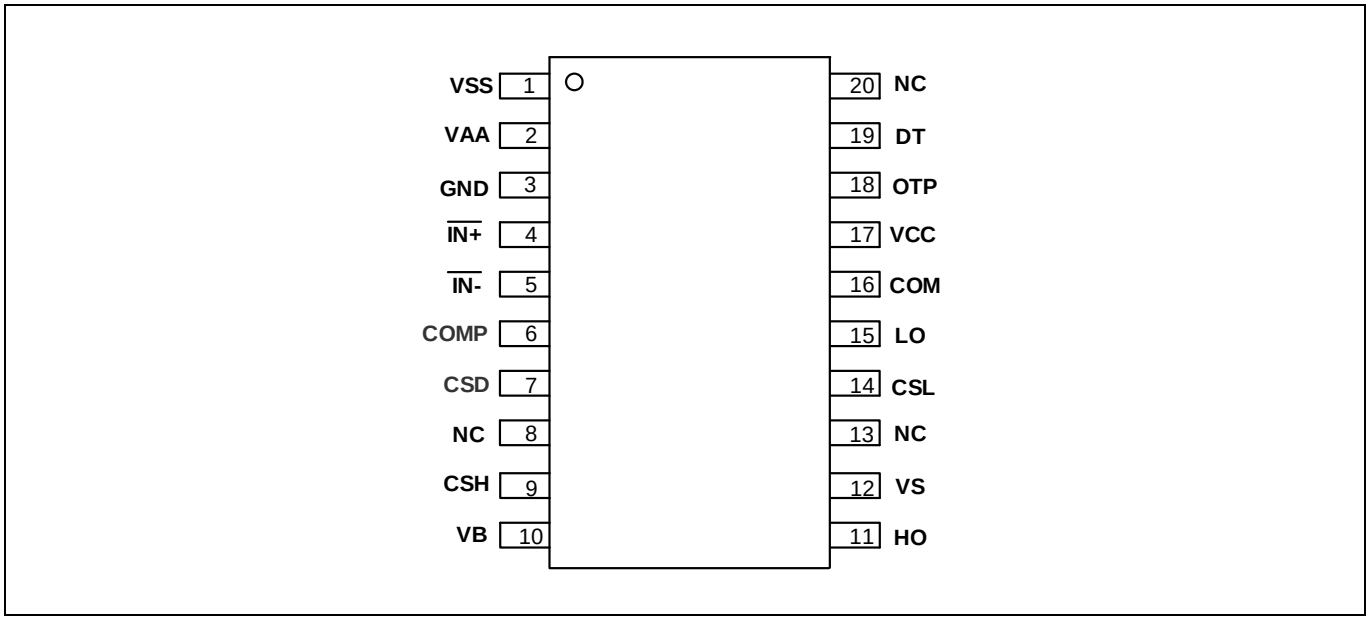

Figure 2 Pin configuration

Table A Pin definitions and functions

Pin	Symbol	Pin type	Function
1	VSS	Input	Floating input negative supply
2	VAA	Input	Floating input positive supply
3	GND	Input	Input reference GND
4	IN+	Input	Non-inverting analog input
5	IN-	Input	Inverting analog input
6	COMP	Input/output	PWM comparator input
7	CSD	Input/output	Protection control
8	NC	-	
9	CSH	Input	High side over current sensing input, referenced to VS
10	VB	Input	High side floating supply
11	HO	Output	High side output
12	VS	Input	High side floating supply return
13	NC	-	
14	CSL	Input	Low side over current sensing input, referenced to COM
15	LO	Output	Low side output
16	COM	Input	Low side gate drive supply return
17	VCC	Input	Low side gate drive supply
18	OTP	Input	OTP sensor input
19	DT	Input	Deadtime program, reference to COM
20	NC	-	

2 Functional block diagram

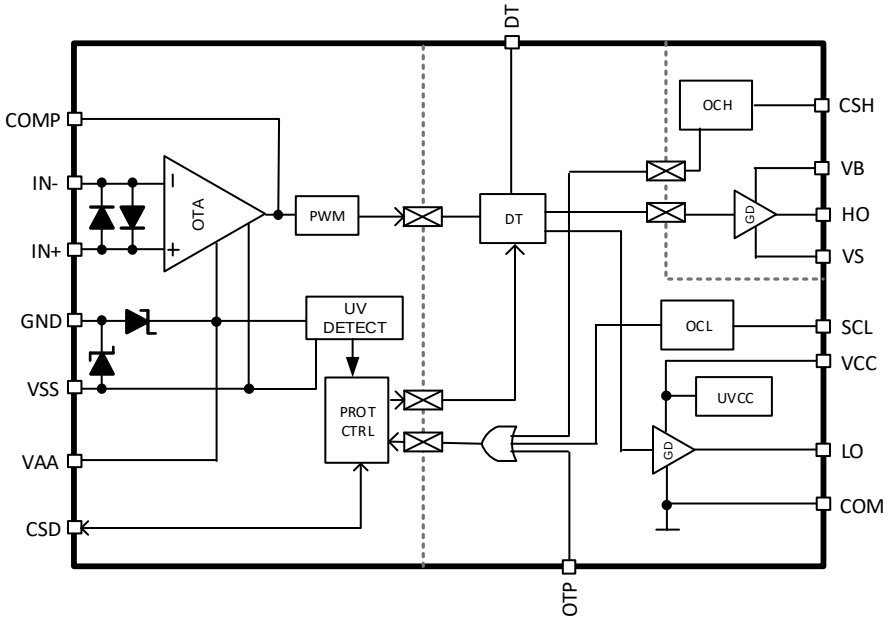

Figure 3 Functional block diagram

3 Qualification Information

Qualification Level		Industrial
Moisture Sensitivity Level		MSL3 (per IPC/JEDEC J-STD-020C)
ESD	**Machine Model**	Class B (per JEDEC standard EIA/JESD22-A115)
	Human Body Model	Class 1B (per EIA/JEDEC standard JESD22-A114)
	Charge Device Model	Class 0B (per EIA/JEDEC standard JESD22-C101)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

4 Characteristics

4.1 Package Characteristic

Symbol	Definition	Min	Max	Units
Pd	Maximum power dissipation @ $T_A \leq +25°C$ ††††	-	1.14	W
Rth_{JA}	Thermal resistance, Junction to ambient ††††	-	65.8	°C/W
T_J	Junction Temperature	-	150	°C
T_S	Storage Temperature	-55	150	°C
T_L	Lead temperature (Soldering, 10 seconds)	-	300	°C

†††† According to JESD51-5. JEDEC still air chamber.

4.2 Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM=VN; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
V_B	High side floating supply voltage	-0.3	415	V
V_S	High side floating supply voltage††	V_{Bn} -15	V_{Bn} +0.3	V
V_{HO}	High side floating output voltage	V_{Sn} -0.3	V_{Bn} +0.3	V
V_{CSH}	CSH pin input voltage	V_{Sn} -0.3	V_{Bn} +0.3	V
V_{CC}	V_{CC} low side fixed supply voltage††	-0.3	15.5	V
V_{LO}	Low side output voltage	-0.3	V_{CC} +0.3	V
V_{AA}	Floating input positive supply voltage††	(See I_{AAZ})	210	V
V_{SS}	Floating input negative supply voltage††	-1 (See I_{SSZ})	V_{AA} +0.3	V
V_{GND}	Floating input supply ground voltage	V_{SS} -0.3	V_{AA} +0.3	V
I_{IN-}	Inverting input current †	-	±3	mA
V_{CSD}	SD pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{COMP}	COMP pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{CLK}	CLK pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{DT}	DT pin input voltage	-0.3	V_{CC} +0.3	V
V_{OTP}	OTP pin input voltage	-0.3	V_{CC} +0.3	V
V_{CSL}	CSL pin input voltage	-0.3	V_{CC} +0.3	V
I_{AAZ}	Floating input positive supply zener clamp current††	-	10	mA
I_{CCZ}	Low side V_{CC} supply zener clamp current††	-	10	mA
I_{BSZ}	Floating supply zener clamp current††	-	10	mA
dV_S/dt	Allowable Vs voltage slew rate	-	50	V/ns
dV_{SS}/dt	Allowable Vss voltage slew rate†††	-	50	V/ms

† IN- contains clamping diode to GND.

†† VAA-VSS, VCC-COM, VB-VS contain internal shunt zener diodes. Note that the voltage ratings of these can be limited by the clamping current.

††† For the rising and falling edges of step signal of 10V. VSS=15V to 200V.

4.3 Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The Vs and COM offset ratings are tested with supplies biased at VAA-VSS=10V, VCC =12V, and VB-VS=12V. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

Symbol	Definition	Min	Max	Units
V_B	High side floating supply absolute voltage	V_{Sn} +10	V_{Sn} +14	V
V_S	High side floating supply offset voltage	(Note1)	400	V
V_{AA}	Floating input supply voltage	V_{SS} + 4.5	V_{SS} + 15	V
I_{AAZ}	Floating input positive supply zener clamp current	1	11	mA
V_{SS}	Floating input supply absolute voltage	0	200	V
V_{HO}	High side floating output voltage	Vs	V_B	V
V_{CC}	Low side fixed supply voltage	10	14	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{GND}	GND pin input voltage	V_{SS}(Note2)	V_{AA}(Note2)	V
V_{IN-}	Inverting input voltage	V_{GND} -0.5(Note2)	V_{GND} +0.5(Note2)	V
V_{CSD}	CSD pin input voltage	V_{SS}	V_{AA}	V
V_{COMP}	COMP pin input voltage	V_{SS}	V_{AA}	V
C_{COMP}	COMP pin phase compensation capacitor to GND	2.2	-	nF
V_{CLK}	CLK pin input voltage	V_{SS}	V_{AA}	V
V_{DT}	DT pin input voltage	0	V_{CC}	V
V_{OTP}	OTP pin input voltage	0	V_{CC}	V
V_{CSH}	CSH pin input voltage	V_{Sn}	V_{Bn}	V
V_{CSL}	CSL pin input voltage	0	V_{CC}	V
dV_{SS}/dt	Allowable V_{SS} voltage slew rate upon power-up(Note3)	-	50	V/ms
f_{SW}	Switching frequency	-	800	kHz
f_{CLK}	CLK frequency(Note4)	-	800	kHz
T_A	Ambient Temperature	-40	125	°C

(Note 1) Logic operational for Vs equal to –5V to +400V. Logic state held for Vs equal to –5V to –VBS.

(Note 2) GND input voltage is limited by IIN-n.

(Note 3) Vss ramps up from 0V to 200V.

(Note 4) The CLK input frequency needs to be within +/-10% of self-oscillating frequency in order to synchronize PWM in a typical self-oscillating application.

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4.4 Electrical Characteristics

VCC= VBS =VDT=12V, VSS=VS=COM =0V, VGND=5V, VAA=10V, CL=1nF and TA=25°C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Side Supply						
UV_{CC+}	Vcc supply UVLO positive threshold	8.4	8.9	9.4	V	
UV_{CC-}	Vcc supply UVLO negative threshold	8.2	8.7	9.2	V	
UV_{CCHYS}	UV_{CC} hysteresis	-	0.2	-	V	
I_{QCC}	Low side quiescent current	-	-	6	mA	$V_{DT}=V_{CC}$
V_{CLAMPL}	Low side zener diode clamp voltage	14.7	15.3	16.2	V	I_{CC}=5mA
High Side Floating Supply						
UV_{BS+}	High side well UVLO positive threshold	8.0	8.5	9.0	V	
UV_{BS-}	High side well UVLO negative threshold	7.8	8.3	8.8	V	
UV_{BSHYS}	UV_{BS} hysteresis	-	0.2	-	V	
I_{QBS}	High side quiescent current	-	-	1	mA	
I_{LKH}	High to Low side leakage current	-	-	50	µA	$V_B=V_S$ =400V
V_{CLAMPH}	High side zener diode clamp voltage	14.7	15.3	16.2	V	I_{BS}=5mA
Floating Input Supply						
UV_{AA+}	V_{AA} floating supply UVLO positive threshold from V_{SS}	8.2	8.7	9.2	V	GND pin floating
UV_{AA-}	V_{AA} floating supply UVLO negative threshold from V_{SS}	7.7	8.2	8.7	V	GND pin floating
UV_{AAHYS}	UV_{AA} hysteresis	-	0.5	-	V	GND pin floating
I_{QAASD}	Floating Input positive quiescent supply current in shutdown mode	-	2	3	mA	V_{CSD} =V_{GND}
I_{QAA0}	Floating Input positive quiescent supply current, positive input	-	4	6	mA	V_{IN-} = VSS+5.2V
I_{QAA1}	Floating Input positive quiescent supply current, negative input	-	3	4	mA	V_{IN-} = VSS+4.8V
I_{QAAST}	Floating Input positive quiescent supply current in start-up mode	-	3	4	mA	V_{CSD} = V_{GND}+2.5V
I_{LKM}	Floating input side to Low side leakage current	-	-	50	µA	V_{AA}=V_{SS}=V_{GND}= 100V
V_{CLAMPM}	Floating supply zener diode clamp voltage	14.7	15.3	16.2	V	I_{AA}=5mA, V_{CSD} =V_{GND}

Characteristics

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Audio Input (GND=0V, V_{AA}=5V, V_{SS}=-5V, COM =V_{CC} =-5V, V_S=CSH=-5V, DT=-5V)						
V_{Os}	Input offset voltage	-18	0	18	mV	
I_{BIN}	Input bias current	-	-	40	nA	
GBW	Small signal bandwidth	-	5 Note 1	-	MHz	C_{COMPn}=2.2nF, Rf=10k, Note 1
V_{COMP}	OTA Output voltage	V_{AA}-1	-	V_{SS}+1	V	
g_m	OTA transconductance	80	200	260	mS	V_{IN-}=10mV
G_V	OTA gain	60	-	-	dB	
V_{Nrms}	OTA input noise voltage	-	250	-	mVrms	BW=20kHz, Resolution BW=22Hz Fig.8
SR	Slew rate	-	±5	-	V/us	C_{COMP}=2.2nF
CMRR	Common-mode rejection ratio	-	60	-	dB	
PSRR	Supply voltage rejection ratio	-	65	-	dB	
PWM Comparator						
Vth_{PWM}	PWM comparator threshold in COMP	-	(V_{AA} – V_{SS})/2	-	V	
f_{OTA}	COMP pin star-up local oscillation frequency	-	0.6	-	MHz	V_{CSD} =V_{GND}+2.5V
Protection						
Vth_{OCL}	Low side OC threshold in V_{CSL}	1.1	1.2	1.3	V	
Vth_{OCH}	High side OC threshold in V_{CSH}	1.1+ Vs	1.2+ Vs	1.3+ Vs	V	Vs=400V
Vth1	CSD pin shutdown release threshold	0.52xV_{AA-GND}	0.68xV_{AA-GND}	0.84xV_{AA-GND}	V	
Vth2	CSD pin self reset threshold	0.26xV_{AA-GND}	0.30xV_{AA-GND}	0.34xV_{AA-GND}	V	
I_{CSD+}	CSD pin discharge current	70	100	130	µA	V_{CSD} = V_{GND} + 2.4V
I_{CSD-}	CSD pin charge current	70	100	130	µA	V_{CSD} = V_{GND} + 2.4V
t_{SSD}	Shutdown propagation delay from V_{CSD} < V_{GND}+ Vth1 to Shutdown	-	140	250	ns	
t_{OCH}	Propagation delay time from V_{CSHn} > Vth_{OCHn} to Shutdown	-	400	500	ns	
t_{OCL}	Propagation delay time from Vsn> Vth_{OCL} to Shutdown	-	270	350	ns	
V_{OTP}	OTP pin input threshold	-	2.8	-	V	
I_{OTP}	OTP bias sourcing current	-	0.6	-	mA	OTP=0V

Characteristics

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Gate Driver						
Io+	Output high short circuit current (Source)	-	0.5	-	A	Vo=0V, PW≤10µS, Note 1
Io-	Output low short circuit current (Sink)	-	0.6	-	A	Vo=12V, PW≤10µS, Note 1
V_{OL}	Low level output voltage LO – COM, HO - VS	-	-	0.1	V	Io=0A
V_{OH}	High level output voltage VCC – LO, VB - HO	-	-	1.4	V	
Ton0	High and low side turn-on propagation delay	-	505	-	ns	V_{DT} = COM
Toff0	High and low side turn-off propagation delay	270	340	410	ns	
Toffskw	Toff skew, Toffhon – Tofflon	-30	0	30	ns	
tr	Turn-on rise time	-	12	25	ns	
tf	Turn-off fall time	-	12	25	ns	
DT1	Deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LnO turn-on (DT_{HO-LO})	130	165	200	ns	V_{DT}>V_{DT1}, V_{DTM}=COM
DT2	Deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LOn turn-on (DT_{HO-LO})	180	225	270	ns	V_{DT1}>V_{DT}> V_{DT2}, V_{DTM}=COM
DT3	Deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LOn turn-on (DT_{HO-LO})	225	280	335	ns	V_{DT2}>V_{DT}> V_{DT3}, V_{DTM}=COM
DT4	Deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HO turn-off to LOn turn-on (DT_{HO-LO})V_{DT}= V_{DT4}	275	340	405	ns	V_{DT}<V_{DT3}, V_{DTM}=COM
V_{DT1}	DT mode select threshold 1	0.51xVcc	0.57xVcc	0.63xVcc	V	V_{DTM}=COM
V_{DT2}	DT mode select threshold 2	0.32xVcc	0.36xVcc	0.40xVcc	V	
V_{DT3}	DT mode select threshold 3	0.21xVcc	0.23xVcc	0.25xVcc	V	

Note 1 Guaranteed by design, but not tested in production.

4.5 Waveform definitions

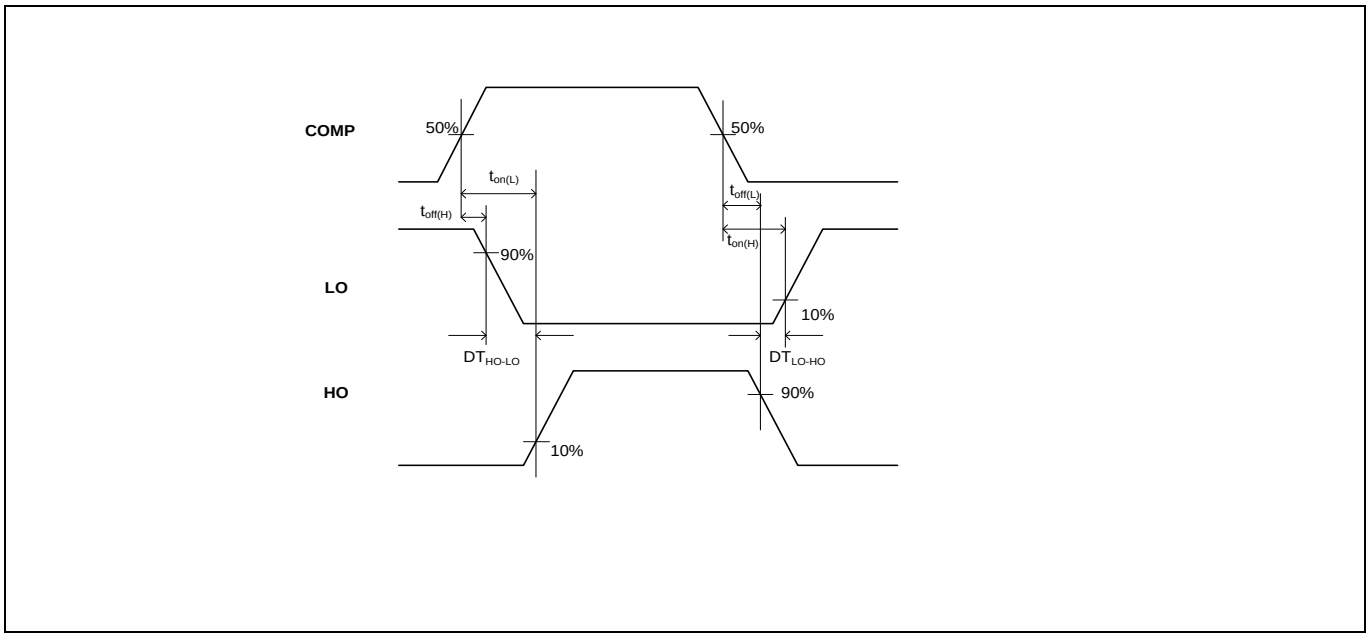

Figure 4 Switching time waveform definitions

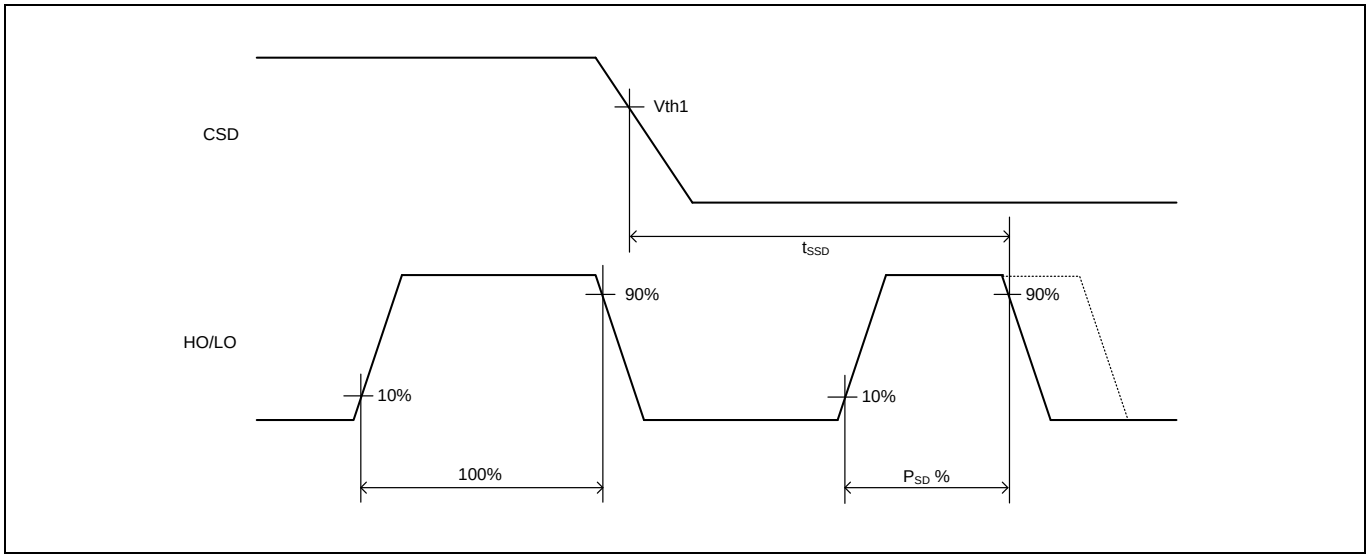

Figure 5 CSD to shutdown waveform definitions

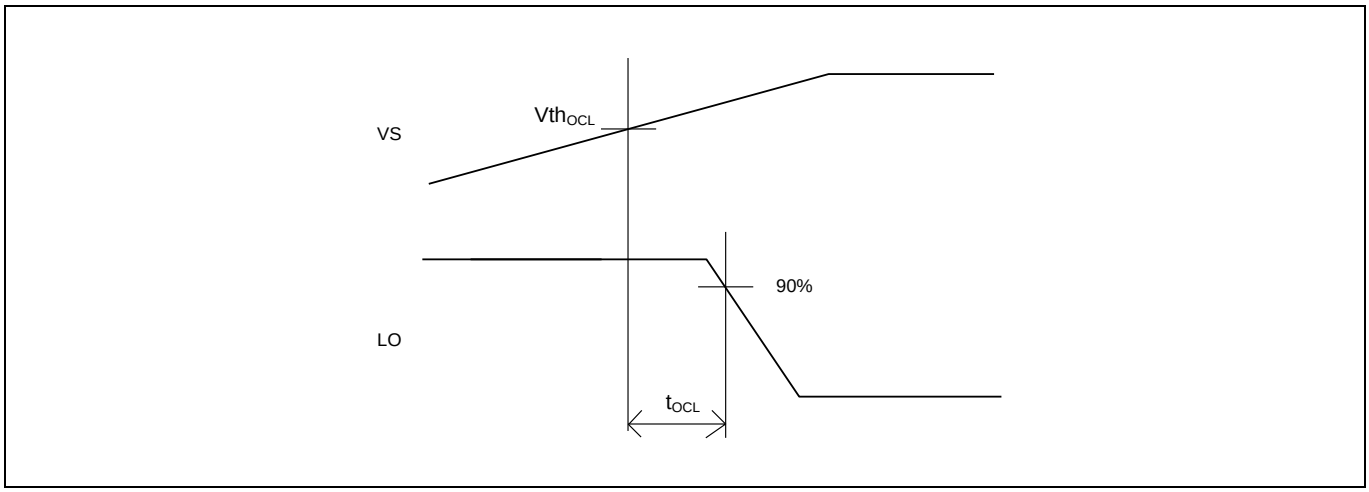

Figure 6 V_S > Vth_{OCL} to shutdown waveform

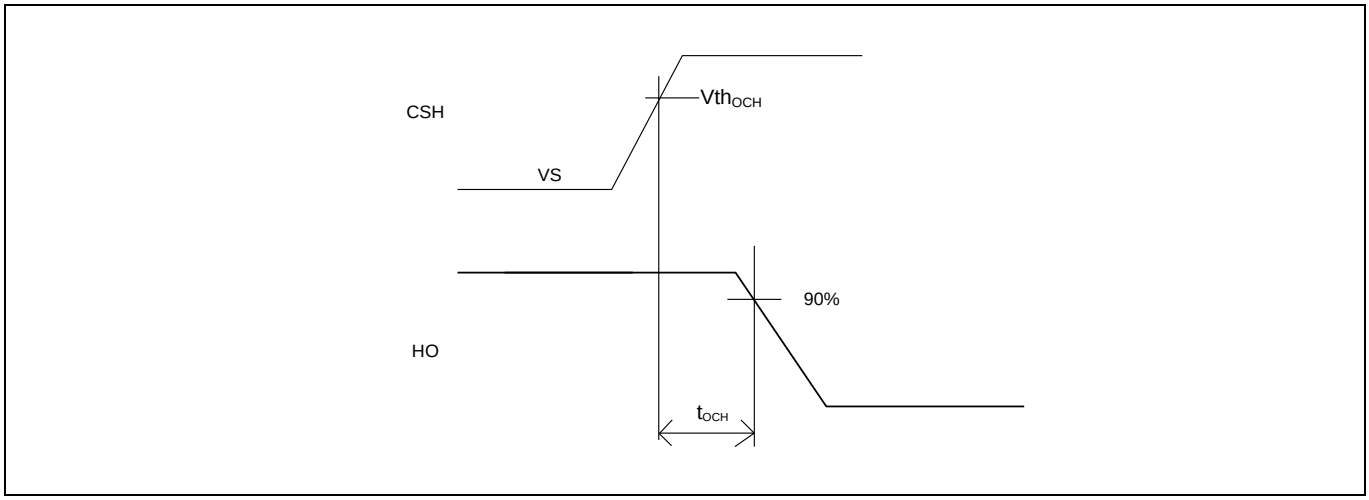

Figure 7 V_{CSH} > Vth_{OCH} to shutdown waveform

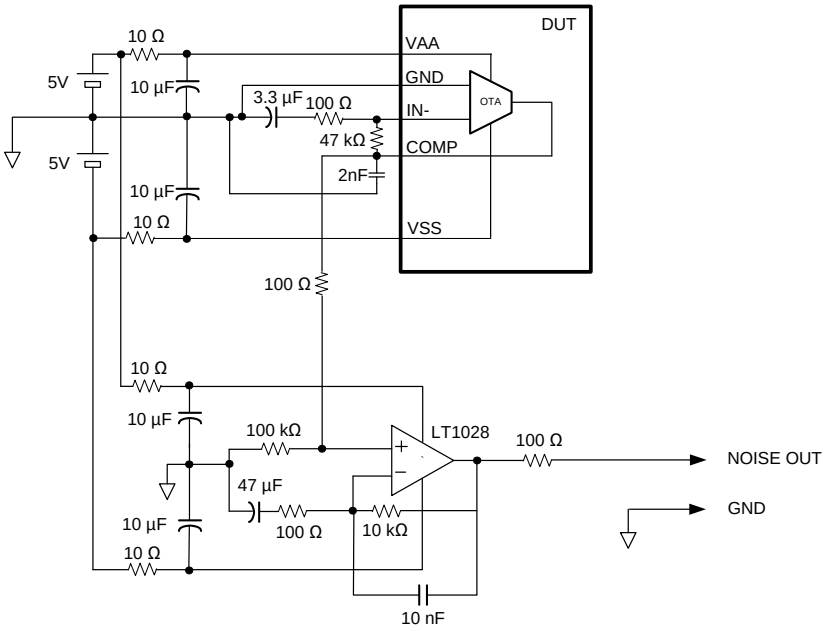

Figure 8 OTA input noise voltage measuring circuit

5 Package dimensions

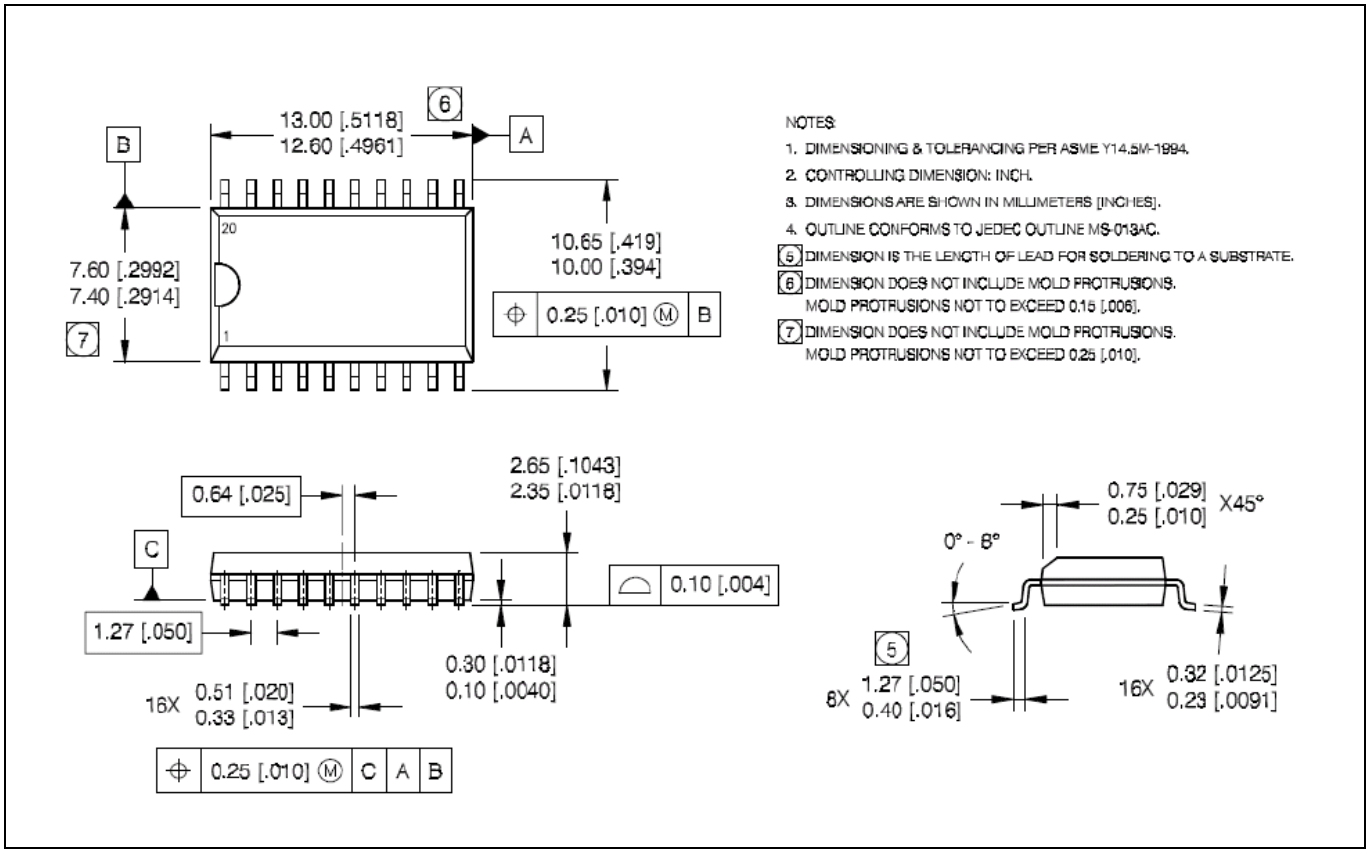

Figure 9 20 Lead SOIC (wide body)

6 Marking

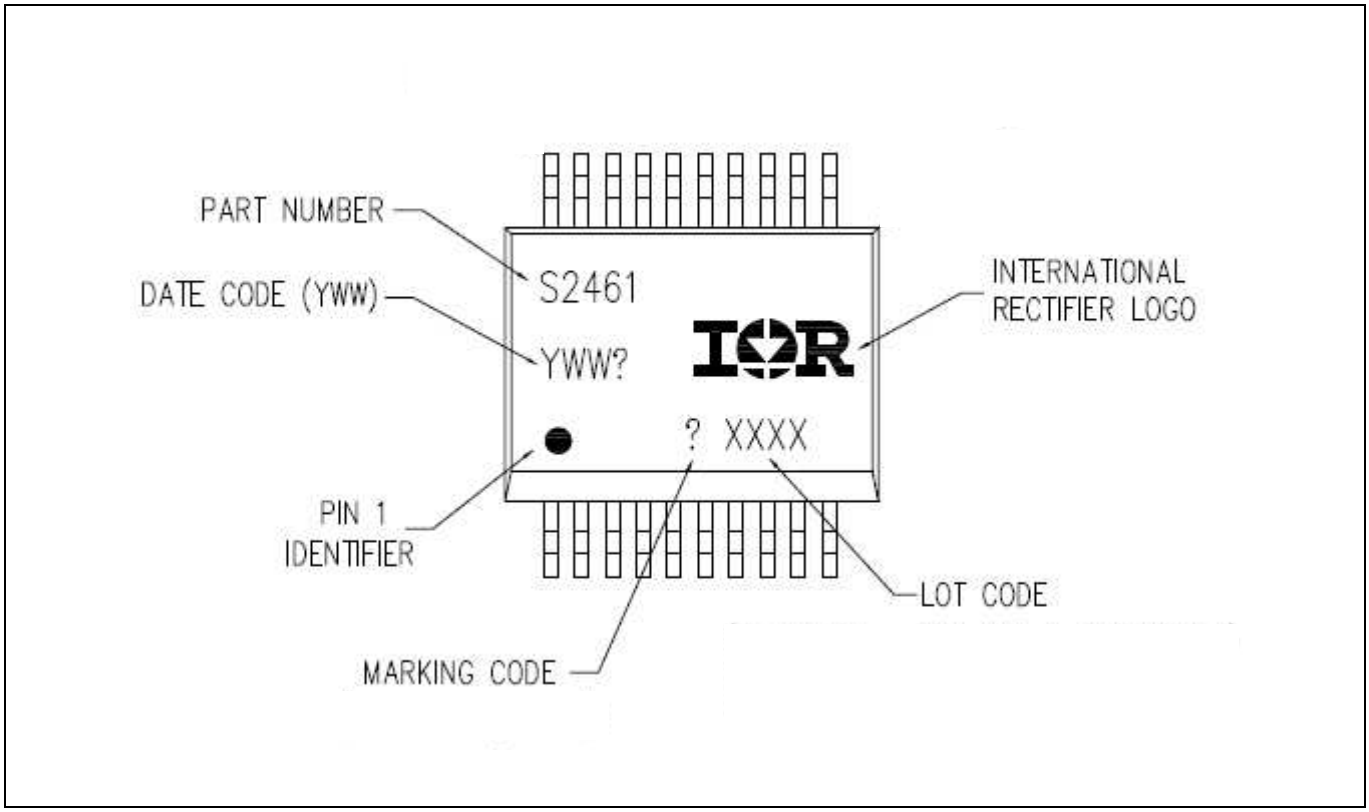

Figure 10 Top marking (laser)

Revision History

IRS2461S

Revision: 2019-06-04, Rev. 2.3

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
1.2	2018-06-26	unified part name to IRS2461S
2.3	2019-06-04	added ton(typ)

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