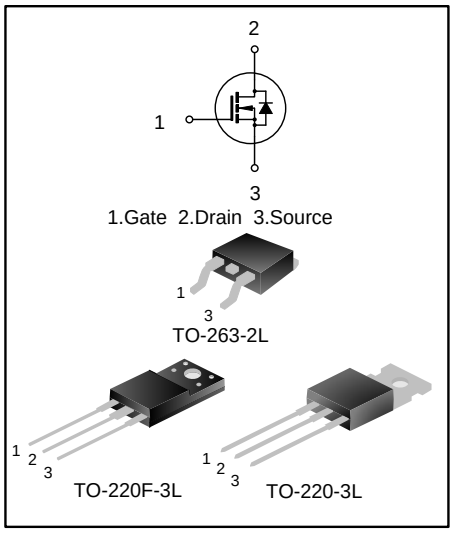
7A, 650V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF7N65T/F/S is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 7A, 650V, $R_{DS(on)(typ.)}$=1.1Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVF7N65F	TO-220F-3L	SVF7N65F	Pb free	Tube
SVF7N65S	TO-263-2L	SVF7N65S	Halogen free	Tube
SVF7N65STR	TO-263-2L	SVF7N65S	Halogen free	Tape & Reel
SVF7N65T	TO-220-3L	SVF7N65T	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C, UNLESS OTHERWISE NOTED)

Characteristics		Symbol	Ratings			Unit
			SVF7N65T	SVF7N65F	SVF7N65S	
Drain-Source Voltage		V_{DS}	650			V
Gate-Source Voltage		V_{GS}	±30			V
Drain Current	T_C = 25°C	I_D	7.0			A
	T_C = 100°C		4.4			
Drain Current Pulsed		I_{DM}	28			A
Power Dissipation(T_C=25°C)		P_D	145	46	120	W
-Derate above 25°C			1.16	0.37	0.96	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	435			mJ
Reverse Diode dv/dt (Note 2)		dv/dt	4.5			V/ns
MOSFET dv/dt Ruggedness (Note 3)		dv/dt	50			V/ns
Operation Junction Temperature Range		T_J	-55～+150			°C
Storage Temperature Range		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVF7N65T	SVF7N65F	SVF7N65S	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.86	2.7	1.04	°C/ W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	62.5	°C/ W

ELECTRICAL CHARACTERISTICS (T_C=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=3.5A	--	1.1	1.4	Ω
Input Capacitance	R_g	f=1.0MHz	--	2.8	--	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHz	--	789	--	pF
Output Capacitance	C_{oss}		--	98	--	
Reverse Transfer Capacitance	C_{rss}		--	9.0	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V, R_G=25Ω, I_D=7.0A (Note 4,5)	--	15	--	ns
Turn-on Rise Time	t_r		--	32	--	
Turn-off Delay Time	$t_{d(off)}$		--	51	--	
Turn-off Fall Time	t_f		--	33	--	
Total Gate Charge	Q_g	V_{DS}=520V, I_D=7.0A, V_{GS}=10V (Note 4,5)	--	21	--	nC
Gate-Source Charge	Q_{gs}		--	4.5	--	
Gate-Drain Charge	Q_{gd}		--	10	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	7.0	A
Pulsed Source Current	I_{SM}		--	--	28	
Diode Forward Voltage	V_{SD}	I_S=7.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=7.0A,V_{GS}=0V, dI_F/dt=100A/μs (Note 4)	--	499	--	ns
Reverse Recovery Charge	Q_{rr}		--	3.0	--	μC

Notes:

1. L=30mH, I_{AS}=5.0A, V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C;
2. V_{DS}=0~400V, I_{SD}<=10A, T_J=25°C;
3. V_{DS}=0~480V;
4. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

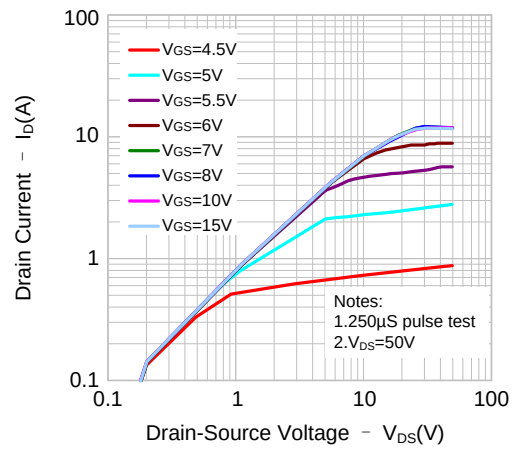


Figure 2. Transfer Characteristics

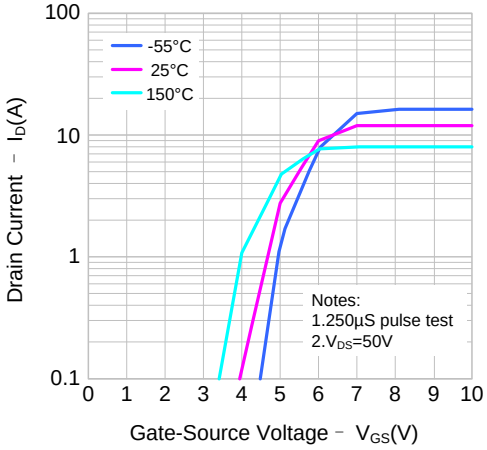


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

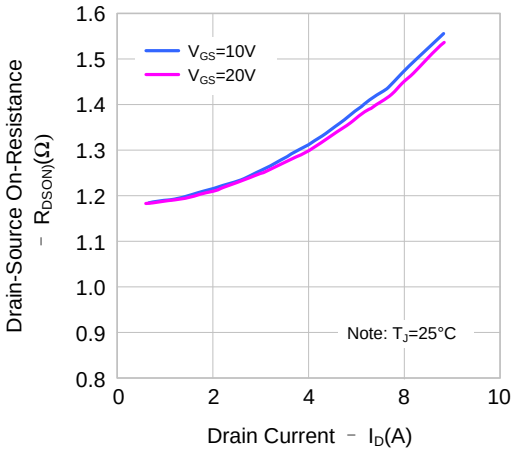


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

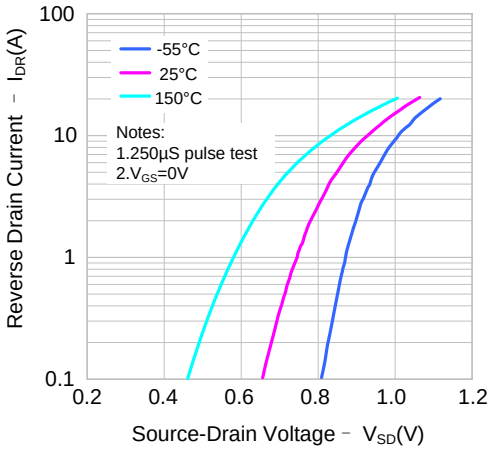


Figure 5. Capacitance Characteristics

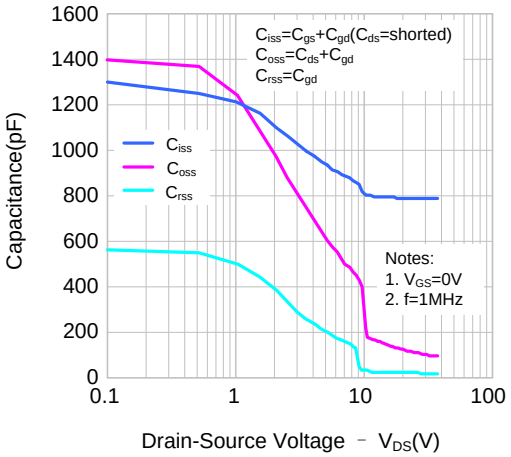
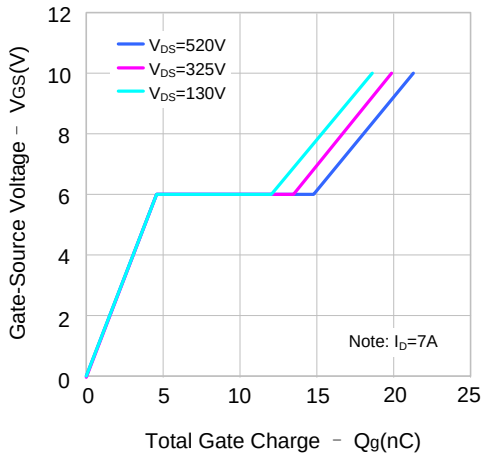


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS (continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

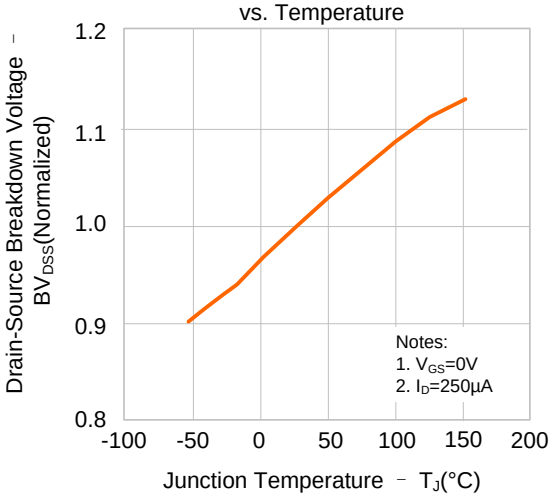


Figure 8. On-resistance Variation vs. Temperature

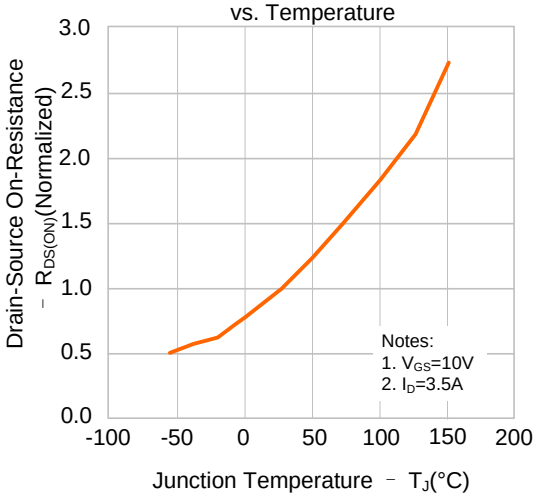


Figure 9-1. Max. Safe Operating Area(SVF7N65F)

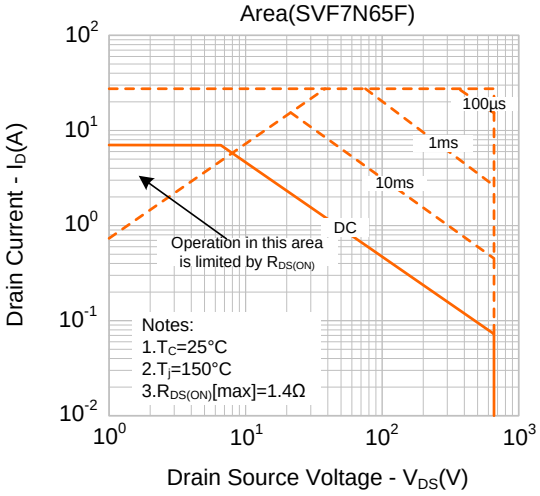


Figure 9-2. Max. Safe Operating Area(SVF7N65S)

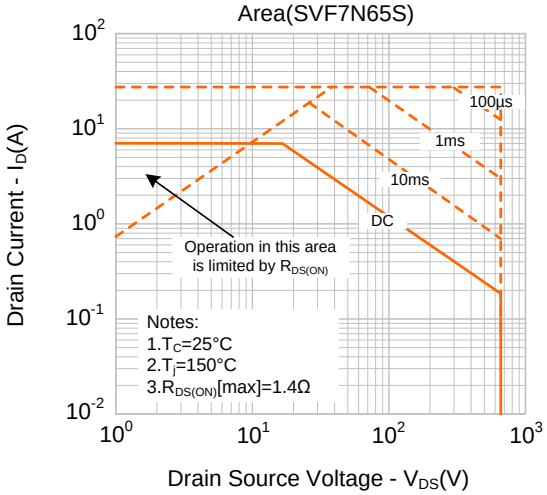


Figure 9-3. Max. Safe Operating Area(SVF7N65T)

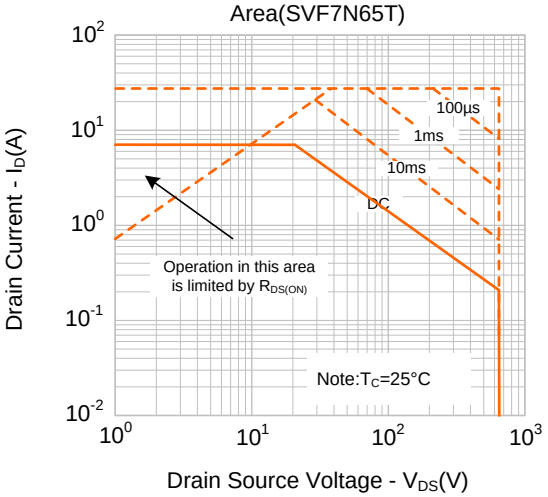
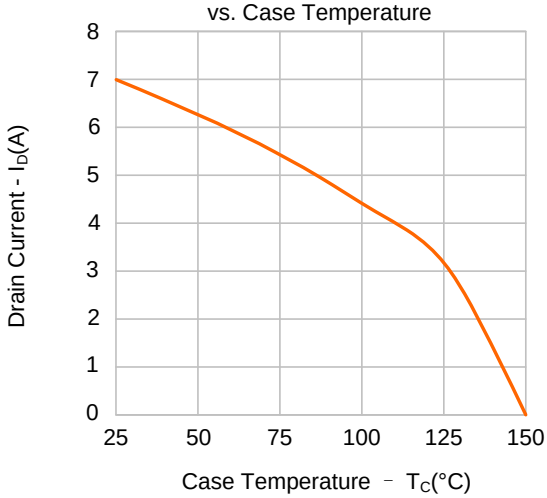
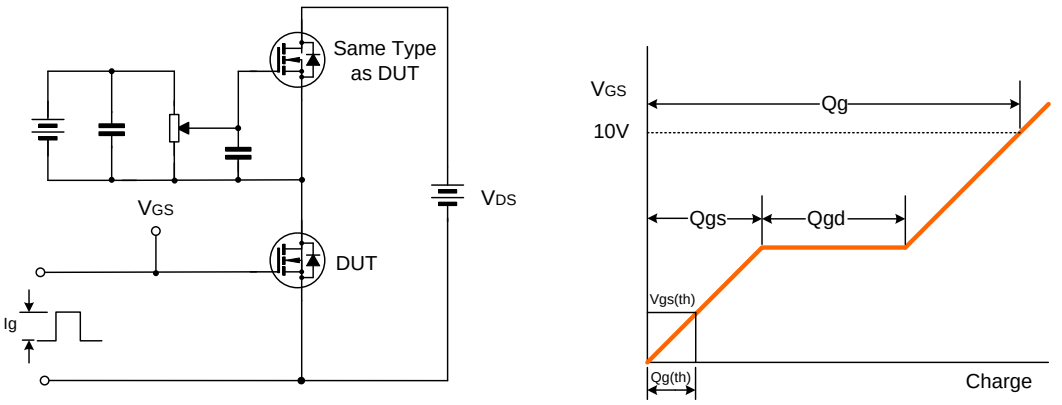


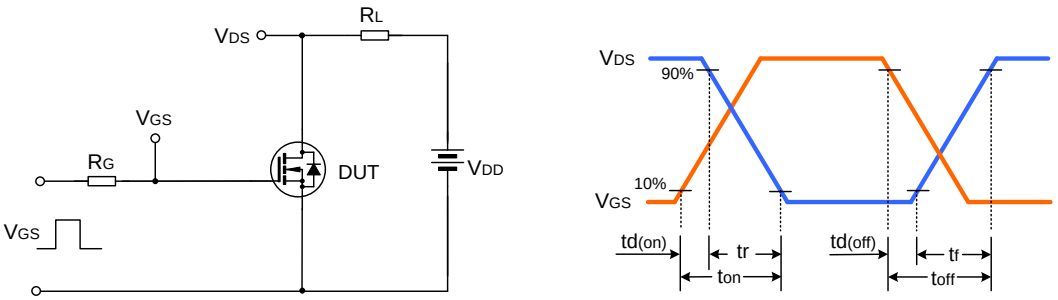
Figure 10. Maximum Drain Current vs. Case Temperature



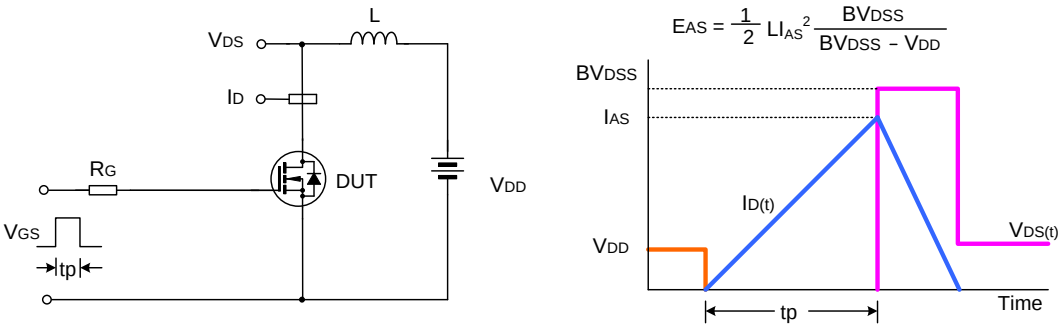
TYPICAL TEST CIRCUIT



Gate Charge Test Circuit & Waveform



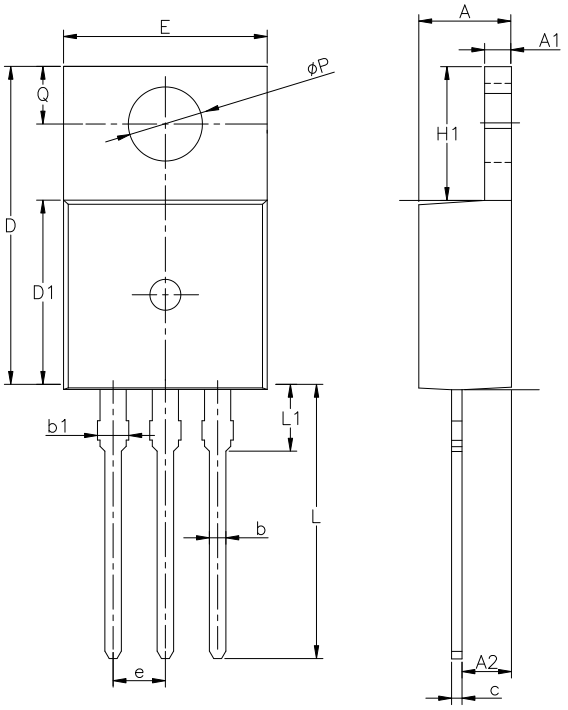
Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform

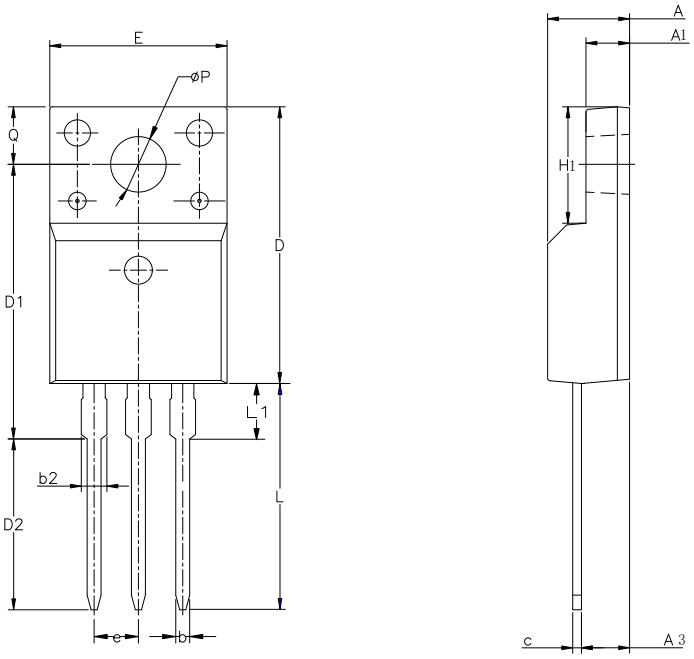
PACKAGE OUTLINE

TO-220-3L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ΦP	3.40	3.70	3.90
Q	2.60	—	3.20

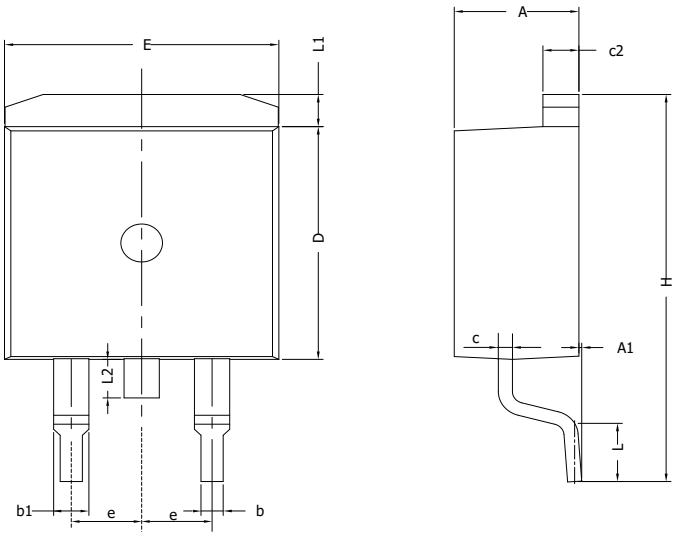
TO-220F-3L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
ΦP	3.00	3.18	3.40
Q	3.05	3.30	3.55

PACKAGE OUTLINE

TO-263-2L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	---	0.60
c2	1.17	1.27	1.37
D	8.50	---	9.35
E	9.80	---	10.45
e		2.54BSC	
H	14.70	---	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	---	---	1.75

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Rev.: 2.9

Revision History:

1. Modify Electrical schematic and TYPICAL TEST CIRCUIT
2. Modify some Characteristics

Rev.: 2.8

Revision History:

1. Delete the package outline of TO-262-3L

Rev.: 2.7

Revision History:

1. Update the package outline of TO-262-3L
2. Add another solid figure of TO-220-3L

Rev.: 2.6

Revision History:

1. Update the package outline of TO-262-3L

Rev.: 2.5

Revision History:

1. Modify Electrical characteristics

Rev.: 2.4

Revision History:

1. Update template
2. Update package outline of TO-262-3L and TO-263-2L
3. Update space diagram of TO-220-3L and Hazardous Substance Control of TO-262-3L

Rev.: 2.3

Revision History:

1. Modify the package information of TO-220F-3L; Modify the package information of TO-220-3L

Rev.: 2.2

Revision History:

1. Modify the thermal characteristics

Rev.: 2.1

Revision History:

1. Modify the ordering information

Rev.: 2.0

Revision History:

1. Modify the ordering information

Rev.: 1.9

Revision History:

1. Change the schematic diagram of MOS

Rev.: 1.8

Revision History:

1. Modify “PACKAGE OUTLINE”

Rev.: 1.7

Revision History:

1. Add the package of TO-263-2L

Rev.: 1.6

Revision History:

1. Add the package of TO-262-3L

Rev.: 1.5

Revision History:

1. Modify the value of Trr and Qrr; Modify the figure 1

Rev.: 1.4

Revision History:

1. Add the halogen free information of SVF7N65F

Rev.: 1.3

Revision History:

1. Modify “ELECTRICAL CHARACTERISTICS” and the capacitance characteristic curve

Rev.: 1.2

Revision History:

1. Modify “PACKAGE OUTLINE”

Rev.: 1.1

Revision History:

1. Modify “ABSOLUTE MAXIMUM RATINGS” and “ELECTRICAL CHARACTERISTICS”

Rev.: 1.0

Revision History:

1. First release