CMOS 4-Bit Microcontroller

TMP47C200BN, TMP47C400BN
TMP47C200BF, TMP47C400BF

The TMP47C200B/400B are high speed and high performance 4-bit single chip microcomputers, integrating ROM, RAM, input / output ports, timer / counters, and a serial interface on a chip. The TMP47C200B/400B are the standard type devices in the TLCS-47 CMOS series. The TMP47C200B/400B are low voltage and high speed 4-bit single chip microcomputer based on the TMP47C200A/400A. The other configurations and functions are same those of the TMP47C200A/400A.

Part No.	ROM	RAM	Package	OTP
TMP47C200BN	2048 × 8-bit	128 × 4-bit	P-SDIP42-600-1.78	TMP47P400VN
TMP47C200BF			P-QFP44-1414-0.80D	TMP47P400VF
TMP47C400BN	4096 × 8-bit	256 × 4-bit	P-SDIP42-600-1.78	TMP47P400VN
TMP47C400BF			P-QFP44-1414-0.80D	TMP47P400VF

Features

◆4-bit single chip microcomputer

◆Instruction execution time: 1.9 μs (at 4.2 MHz)

◆90 basic instructions
- Table look-up instructions
- 5-bit to 8-bit data conversion instruction

◆Subroutine nesting: 15 levels max.

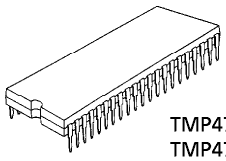
◆6 interrupt sources (External: 2, Internal: 4)
All sources have independent latches each, and multiple interrupt control is available.

◆I/O port (36 pins)
- Input 2 ports 5 pins
- Output 2 ports 8 pins
- I/O 6 ports 23 pins

◆Interval Timer

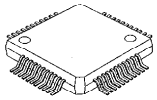
◆Two 12-bit Timer/Counters
Timer, event counter, and pulse width measurement mode

P-SDIP42-600-1.78



TMP47C200BN
TMP47C400BN
TMP47P400VN

P-QFP44-1414-0.80D



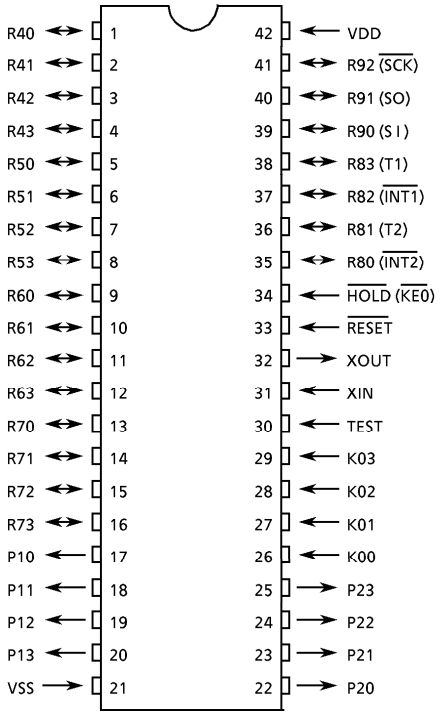
TMP47C200BF
TMP47C400BF
TMP47P400VF

000707EBA1

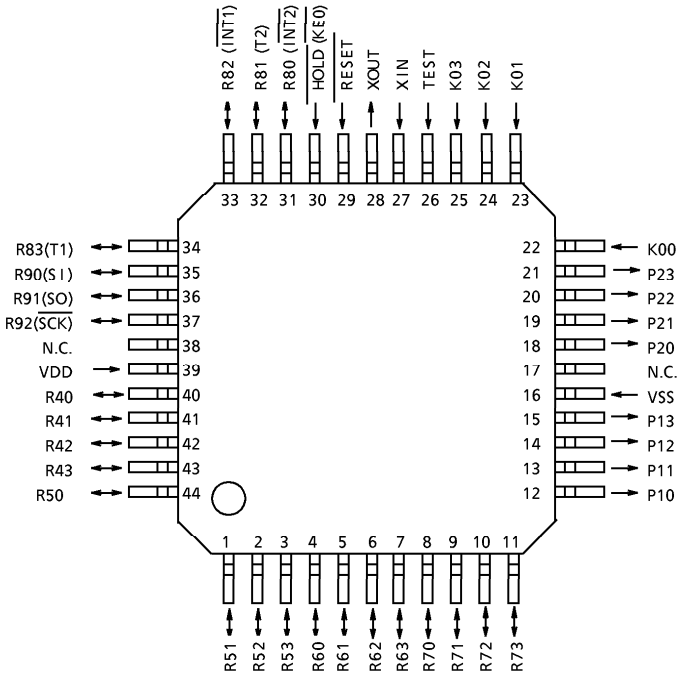
◆Serial Interface with a 4-bit buffer
External/internal clock, and leading/trailing edge shift mode
◆High current outputs
LED direct drive capability (typ. 30 mA × 8 bits)
◆Hold function
Battery / Capacitor back-up
◆Real Time Emulator: BM4721A

Pin Assignments (Top View)

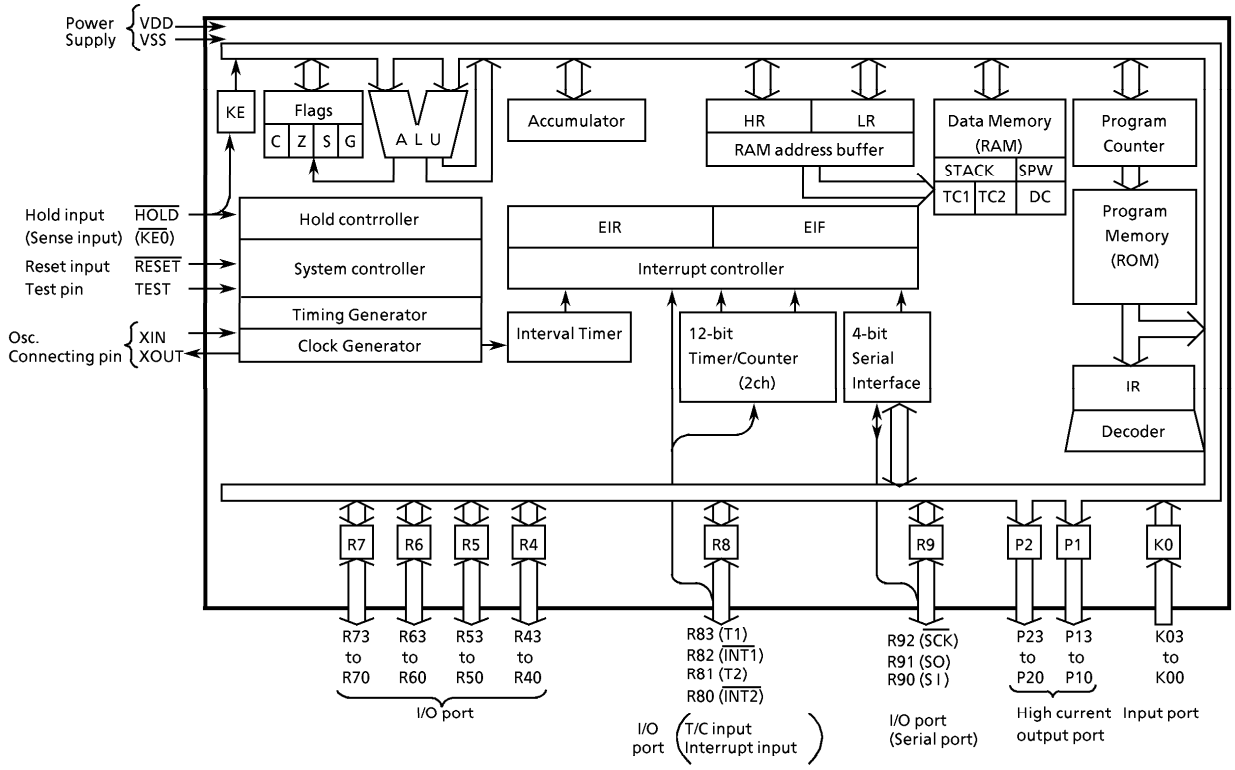
(1) P-SDIP42-600-1.78



(2) P-QFP44-1414-0.80D



Block Diagram



Pin Function

Pin Name	Input / Output	Functions	
K03 to K00	Input	4-bit input port	
P13 to P10	Output	4-bit output port with latch. 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL] .	
P23 to P20			
R43 to R40	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1". Every bit data is possible to be set, cleared and tested by the bit manipulation instruction of the L-register indirect addressing.	
R53 to R50			
R63 to R60			
R73 to R70			
R83 (T1)	I/O(Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 1 input
R92 ($\overline{SCK}$)	I/O(I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O(Output)		Serial data output
R90 (SI)	I/O(Input)		Serial data input
XIN	Input	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input(Input)	Hold request/release signal input	Sense input
TEST	Input	Test pin for shipping. Be opened or fixed to low level.	
VDD	Power Supply	+ 5 V	
VSS		0 V (GND)	

Operational Description

1. System Configuration

◆ Internal CPU Function
- 2.1 Program Counter (PC)
- 2.2 Program Memory (ROM)
- 2.3 H Register, L Register
- 2.4 Data Memory (RAM)
  - Stack
  - Stack Pointer Word (SPW)
  - Data Counter (DC)
- 2.5 ALU, Accumulator
- 2.6 Flags
- 2.7 System controller
- 2.8 Interrupt Controller
- 2.9 Reset Circuit

◆ Peripheral Hardware Function
- 3.1 I/O Ports
- 3.2 Interval Timer
- 3.3 Timer / Counters (TC1, TC2)
- 3.4 Serial Interface

Concerning the above component parts, the configuration and functions of hardwares are described.

2. Internal CPU Function

2.1 Program Counter (PC)

The program counter is a 12-bit binary counter which indicates the address of the program memory storing the next instruction to be executed. Normally, the PC is incremented by the number of bytes of the instruction every time it is fetched. When a branch instruction or a subroutine instruction has been executed or an interrupt has been accepted, the specified values listed in Table 2-1 are set to the PC. The PC is initialized to "0" during reset.

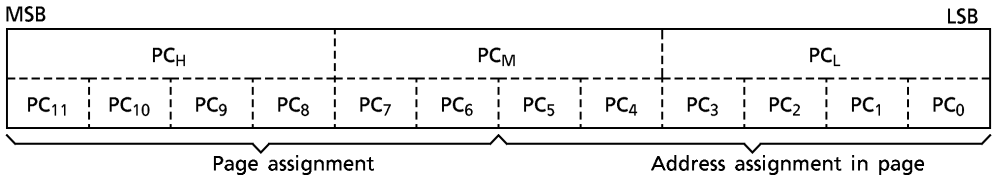


Figure 2-1. Configuration of program counter

The PC can directly address a 4096-byte address space. However, with the short branch and subroutine call instructions, the following points must be considered:

(1) Short branch instruction [BSS a]

In [BSS a] instruction execution, when the branch condition is satisfied, the value specified in the instruction is set to the lower 6 bits of the PC. That is, [BSS a] becomes the in-page branch instruction. When [BSS a] is stored at the last address of the page, the upper 6 bits of the PC point the next page, so that branch is made to the next page.

(2) Subroutine call instruction [CALL a]

In [CALL a] instruction execution, the contents of the PC are saved to the stack then the value specified in the instruction is set to the PC. The address which can be specified by the instruction consists of 11 bits and the most significant bit of the PC is always "0". Therefore, the entry address of the subroutine should be within an addrress range of 000_H through $7FF_H$.

Table 2-1. Status change of program counter

Instruction or Operation		Condition		Program Counter (PC)											
				PC_{11}	PC_{10}	PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC3	PC_2	PC_1	PC_0
Execution of Instruction	BS a	SF = 1 (Branch condition is satisfied)		Immediate data specified by the instruction											
		SF = 0 (Branch condition is not satisfied)		+ 2											
	BSS a	SF = 1	Lower 6-bit address ≠ 111111	Hold						Immediate data specified by the instruction					
			Lower 6-bit address = 111111 (last address in page)	+ 1						Immediate data specified by the instruction					
		SF = 0		+ 1											
	CALL a			0	Immediate data specified by the instruction										
	CALLS a			0	0	0	0	The data generated by the immediate data specified by the instruction					1	1	0
	RET			The return address restored from stack											
	RETI			The return address restored from stack											
	Others			Incremented by the number of bytes in the instruction											
Interrupt acceptance				0	0	0	0	0	0	0	0	Interrupt vector			0
Reset				0	0	0	0	0	0	0	0	0	0	0	0

2.2 Program Memory (ROM)

Programs and fixed data are stored in the program memory. The instruction to be executed next is read from the address indicated by the contents of the PC.

The fixed data can be read by using the table look-up instructions or 5-bit to 8-bit data conversion instruction.

(1) Table look-up instructions

[LDL A, @DC], [LDH A, @DC+]

The table look-up instructions read the lower and upper 4 bits of the fixed data stored at the address specified in the data counter (DC) to place them into the accumulator. [LDL A, @DC] instruction reads the lower 4 bits of fixed data, and [LDH A, @DC+] instruction reads the upper 4 bits.

The DC is a 12-bit register, allowing it to address the entire program memory space.

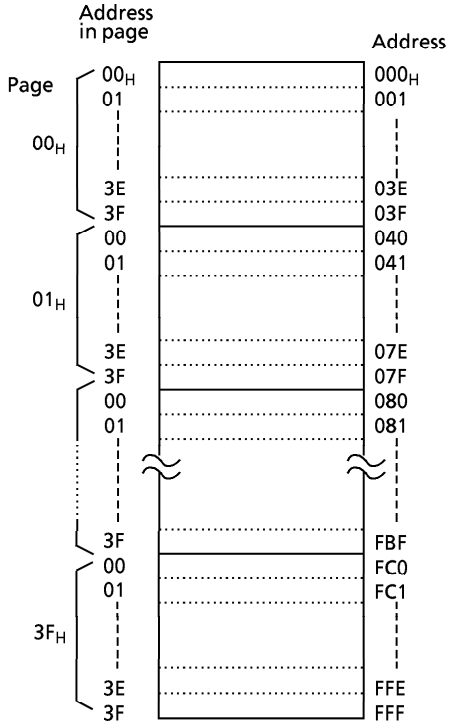


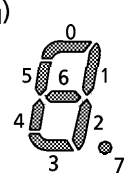
Figure 2-2. Configuration of program memory

(2) 5-bit to 8-bit data conversion instruction [OUTB @HL]

The 5-bit to 8-bit data conversion instruction reads the fixed data (8 bits) from the data conversion table in the program memory to output the upper 4 bits to port P2 and the lower 4 bits to port P1. The table is located in the last 32-byte space (addresses,$7E0_H$ through $7FF_H$ for the TMP47C200B, $FE0_H$ through FFF_H for the TMP47C400B) in the program memory with the lower address consisting of the 5 bits obtained by concatenating the contents of the data memory specified by the HL register pair and the content of the carry flag. This instruction is usable for such applications as converting BCD data into an output code to the 7-segment display elements.

Example: The following shows that the BCD data at address $2F_H$ in the data memory is converted into the 7-segment code (e.g., anode common LED) to be output to ports P2 and P1.

```
LD      HL, #2FH  ;  HL←2FH (Data memory address is set)
TEST    CF        ;  CF←0 (The table is specified at addresses FE0H - FEFH)
OUTB    @HL       ;  Ports P2, P1←fixed data
  ⋮
ORG     FE0H      ;  Data conversion table
DATA    0C0H, 0F9H, 0A4H, 0B0H, 99H, 92H, 82H, 0D8H, 80H, 98H
```

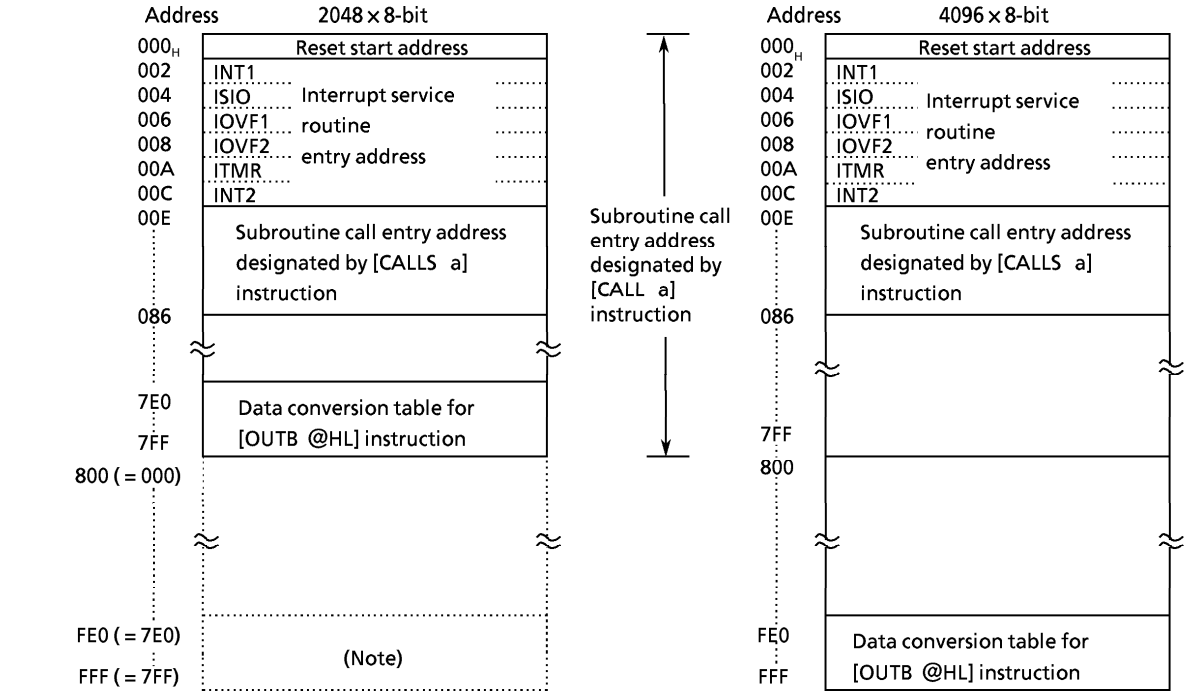


2.2.1 Program Memory Map

Figure 2-3 shows the program memory map. Address 000_H - 086_H and $FE0_H$ - FFF_H (000_H - 086_H and $7E0_H$ - $7FF_H$ for the TMP47C200B) of the program memory are also used for special purposes.

2.2.2 Program Memory Capacity

The TMP47C200B has 2048 × 8 bits (addresses 000_H through $7FF_H$) of program memory (mask ROM), the TMP47C400B has 4096 × 8 bits (addresses 000_H through FFF_H).



Note: When the piggyback is used, the address from $FE0_H$ to FFF_H are used as the data conversion table area.

(a) TMP47C200B (b) TMP47C400B

Figure 2-3. Program memory map

On the TMP47C200B, no physical program memory exists in the address range 800_H through FFF_H. However, if this space is accessed by program, the most significant bit of each address is always regarded as "0" and the contents of the program memory corresponding to the address 000_H through $7FF_H$ are read. For example, when outputting the data at address $FF3_H$ are read to ports by the [OUTB @HL] instruction, the data at address $7F3_H$ is actually read. That is, on the TMP47C200B, the conversion table is located in the address space $7E0_H$ through $7FF_H$. When evaluating the TMP47C200B by using the piggyback chip, however, the conversion table must be allocated in the memory location addressed $FE0_H$ through FFF_H also.

2.3 H Register and L Register

The H register and the L register are 4-bit general registers. They are also used as a register pair (HL) for the data memory (RAM) addressing pointer. The RAM consists of pages, each page being 16 words long (1word = 4bits). The H register specifies a page and the L register specifies an address in the page.

The L register has the auto-post-increment/decrement capability, implementing the execution of composite instructions. For example, [ST A, @HL +] instruction automatically increments the contents of the L register after data transfer.

During the execution of [SET @L], [CLR @L], or [TEST @L] instructions, the L register is also used to specify the bits corresponding to I/O port pins R73 through R40 (the indirect addressing of port bits by the L register).

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 7	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin	– 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1 and P2	30	mA
	I_{OUT2}	Ports R4 through R9	3.2	
Output Current (Total)	ΣI_{OUT1}	Ports P1 and P2	120	mA
Power Dissipation [Topr = 70°C]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Opeating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		In the Normal operating mode	2.7	6.0	V
			In the HOLD operating mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 2.7 to 6.0 V	0.4	4.2	MHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Input voltage V_{IH3}, V_{IL3}: In the SLOW or HOLD mode.

DC Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I_{IN2}	Open drain output ports					
Input Low Current	I_{IL}	Push-pull output ports	V_{DD} = 5.5 V, V_{IN} = 0.4 V	–	–	– 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Open drain output ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
Output High Voltage	V_{OH}	Push-pull output ports	V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	–	–	V
Output Low Voltage	V_{OL2}	Except XOUT and ports P1 and P2	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Output Low Current	I_{OL1}	Ports P1 and P2	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	30	–	mA
Supply Current (in the Normal operating mode)	I_{DD}		V_{DD} = 5.5 V, fc = 4 MHz	–	2	4	mA
			V_{DD} = 3.0 V, fc = 4 MHz	–	1	2	
Supply Current (in the HOLD operating mode)	I_{DDH}		V_{DD} = 5.5 V	–	0.5	10	μA

Note 1: Typ. values show those at T_{opr} = 25°C, V_{DD} = 5 V.

Note 2: Input Current I_{IN1}: The current through resistor is not included, when the pull-up/pull-down resistor is contained.

Note 3: Supply Current: V_{IN} = 5.3 V / 0.2 V

The port K0 with the pull-up/pull-down resistor is open. The voltage applied to the port R4-R9 is within the range V_{IL} or V_{IH}.

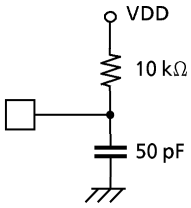
AC Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7 to 6.0 V, Topr = – 30 to 70°C)

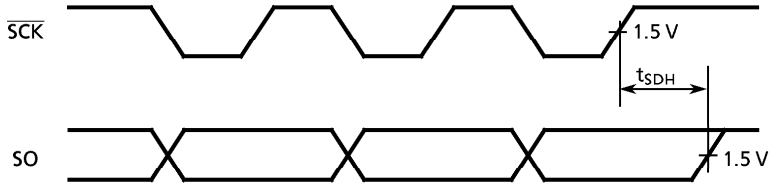
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Instruction Cycle Time	t_{cy}		1.9	–	20	μs
High level Clock pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low level Clock pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		0.5 tcy – 0.3	–	–	μs

Note: Shift data Hold Time:

External circuit for pins $\overline{SCK}$ and SO



Serial port (completed of transmission)



Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 2.7 to 6.0 V, Topr = – 30 to 70°C)

(1) 4 MHz

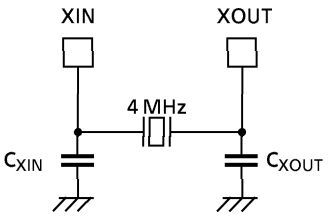
Ceramic Resonator

CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30 pF

KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30 pF

Crystal Oscillator

204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20 pf

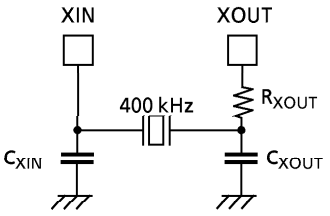


(2) 400 kHz

Ceramic Resonator

CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220 pF, R_{XOUT} = 6.8 kΩ

KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100 pF, R_{XOUT} = 10 kΩ

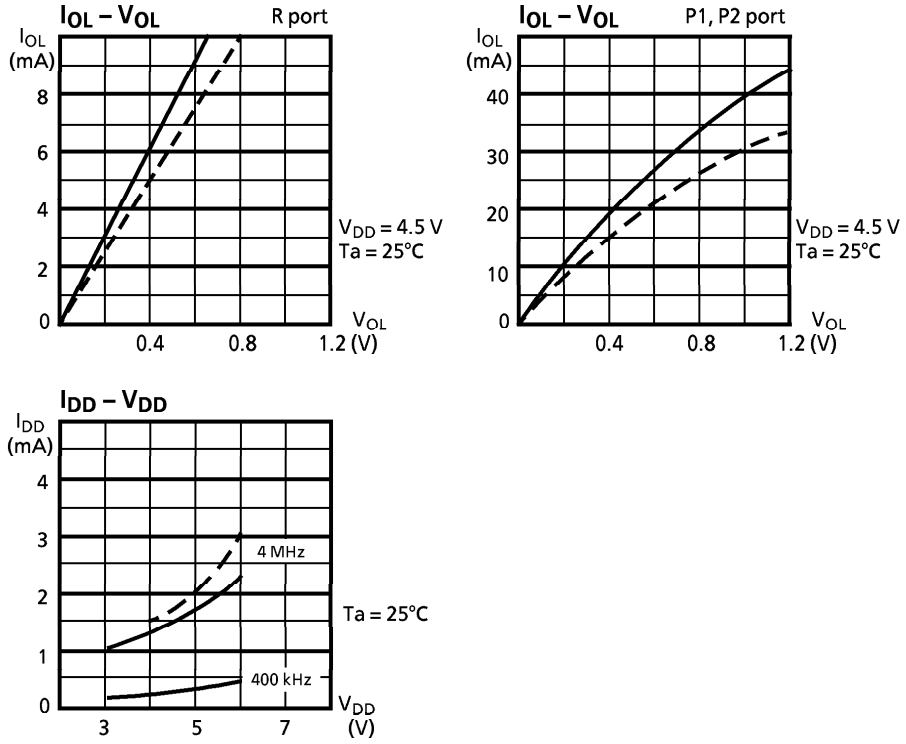


* Difference compared with the TMP47C200A/400A

The TMP47C200B/400B is different from the TMP47C200A/400A with respect to the following spec points.

Parameter	Symbol	Condition	TMPTMP47C200A/400A			TMPTMP47C200B/400B			Unit
			Min	Typ.	Max	Min	Typ.	Max	
Supply Voltage	V_{DD}	In the Normal operating mode	4.5	–	6.0	2.7	–	6.0	V
		In the HOLD operating mode	2.0	–		2.0	–		
Supply Current (in the Normal operating mode)	I_{DD}	V_{DD} = 5.5 V, fc = 4 MHz	–	3	6	–	2	4	mA
		V_{DD} = 3.0 V, fc = 4 MHz	–	–	–	–	1	2	
Clock Frequency	fc	V_{DD} = 2.7 to 6.0 V	–	–	–	0.4	–	4.2	MHz
		V_{DD} = 4.5 to 6.0 V	0.4	–	4.2	–	–	–	
Output Low Current	I_{OL1}	V_{DD} = 4.5 V V_{OL} = 1.0 V	–	20	–	–	30	–	mA

Typical Characteristics



Note: Solid line: TMPTMP47C200B/400B
Rough dotted line: TMPTMP47C200A/400A

Typical Characteristics