2x20W Stereo Class-D Audio Amplifier with Power Limit

Features

- Single supply voltage
  4.5V ~ 26V for loudspeaker driver
  Built-in LDO output 5V for others
- Loudspeaker power from 24V supply
  BTL Mode: 20W/CH into 8Ω @<1% THD+N
  PBTL Mode: 40W/CH into 4Ω @<10% THD+N
- Loudspeaker power from 12V supply
  BTL Mode: 10W/CH into 8Ω @10% THD+N
- 88% efficient Class-D operation eliminates need for heat sink
- Differential inputs
- Four selectable, fixed gain settings
- Internal oscillator
- Short-Circuit protection with auto recovery option
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Adjustable power limit function for speaker protection
- Output DC detection for speaker protection
- Filter-Free operation
- Over temperature protection with auto recovery
- Superior EMC performance

Applications

- TV audio
- Boom-Box
- Powered speaker
- Monitors
- Consumer Audio Equipment

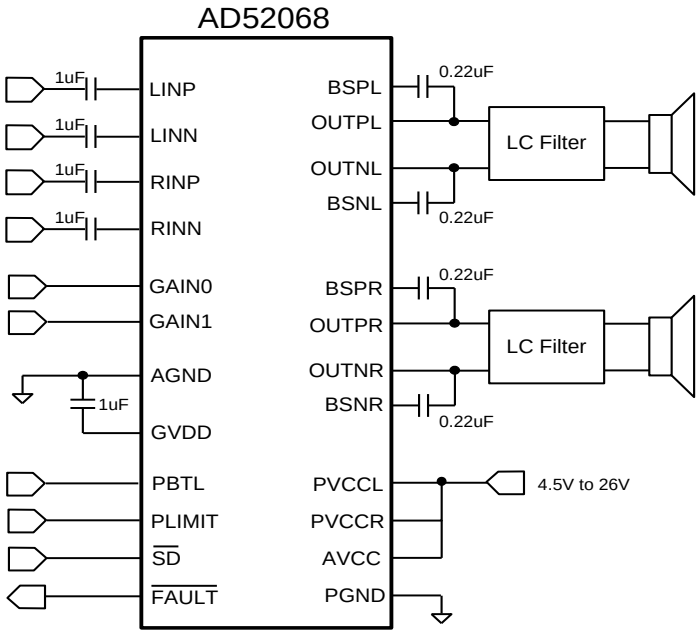
Description

The AD52068 is a high efficiency stereo class-D audio amplifier with adjustable power limit function. The loudspeaker driver operates from 4.5V~26V supply voltage and analog circuit operates at 5V supply voltage. It can deliver 20W/CH output power into 8Ω loudspeaker within 1% THD+N at 24V supply voltage and without external heat sink when playing music.

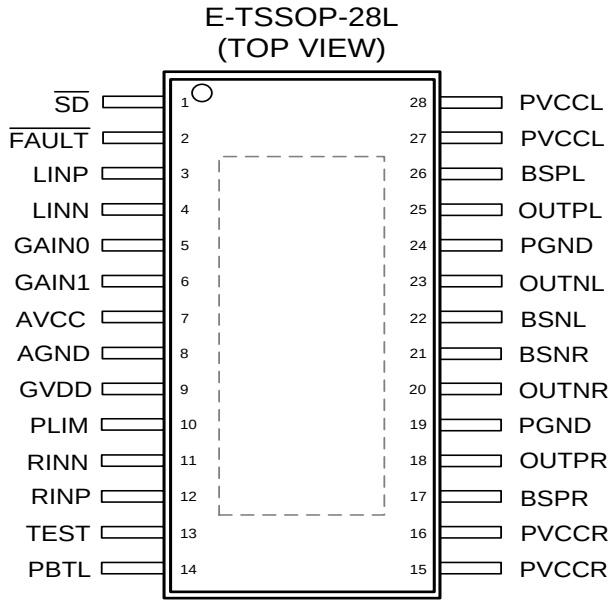
AD52068 provides parallel BTL (Mono) application, and it can deliver 40W into 4Ω loudspeaker at 24V supply voltage. The adjustable power limit function allows user to set a voltage rail lower than half of 5V to limit the amount of current through the speaker.

Output DC detection prevents speaker damage from long-time current stress. AD52068 provides superior EMC performance for filter-free application. The output short circuit and over temperature protection include auto-recovery feature.

Simplified Application Circuit



Pin Assignments



Pin Description

NAME	E-TSSOP -28L	TYP	DESCRIPTION
$\overline{SD}$	1	I	Shutdown signal for IC (low = disabled, high = operational). Voltage compliance to AVCC.
$\overline{FAULT}$	2	O	Open drain output used to display short circuit or dc detect fault. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting FAULTB pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling AVCC.
LINP	3	I	Positive audio input for left channel. Biased at 1/10 of PVCC supply voltage.
LINN	4	I	Negative audio input for left channel. Biased at 1/10 of PVCC supply voltage.
GAIN0	5	I	Gain select least significant bit. Voltage compliance to AVCC.
GAIN1	6	I	Gain select most significant bit. Voltage compliance to AVCC.
AVCC	7	P	Analog supply.
AGND	8	P	Analog signal ground. Connect to the thermal pad.
GVDD	9	O	5V regulated output, also used as supply for PLIMIT function.
PLIMIT	10	I	Power limit level adjustment. Connect a resistor divider from GVDD to GND to set power limit. Give V(PLIMIT) <2.4V to set power limit level. Connect to GVDD (>2.4V) or GND to disable power limit function.
RINN	11	I	Negative audio input for right channel. Biased at 1/10 of PVCC supply voltage.
RINP	12	I	Positive audio input for right channel. Biased at 1/10 of PVCC supply voltage.
TEST	13	I	Test mode pin. Tie this pin to “High” is prohibited, keep it floating during normal operating.

PBTL	14	I	Parallel BTL mode switch, high for parallel BTL output. Voltage compliance to AVCC.
PVCCR	15,16	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
BSPR	17	I	Bootstrap I/O for right channel, positive high side FET.
OUTPR	18	O	Class-D H-bridge positive output for right channel.
PGND	19	P	Power ground for the H-bridges.
OUTNR	20	O	Class-D H-bridge negative output for right channel.
BSNR	21	I	Bootstrap I/O for right channel, negative high side FET.
BSNL	22	I	Bootstrap I/O for left channel, negative high side FET.
OUTNL	23	O	Class-D H-bridge negative output for left channel.
PGND	24	P	Power ground for the H-bridges.
OUTPL	25	O	Class-D H-bridge positive output for left channel.
BSPL	26	I	Bootstrap I/O for left channel, positive high side FET.
PVCCL	27,28	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
Thermal Pad		P	Must be soldered to PCB's ground plane.

Ordering Information

Product ID	Package	Packing	Comments
AD52068-QG28NRR	E-TSSOP 28L	2500 Units / Reel 2500 Units / Small Box	Green

Available Package

Package Type	Device No.	θ_{JA}(℃/W)	θ_{JT}(℃/W)	Ψ_{JT}(℃/W)	Exposed Thermal Pad
E-TSSOP 28L	AD52068	28	27.1	1.33	Yes (Note 1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is necessary.

Note 1.2: θ_{JA} is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is simulated using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{JT} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

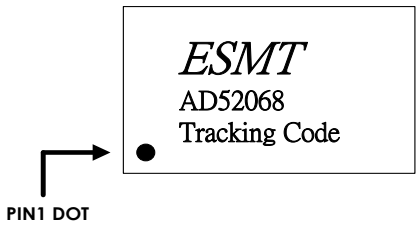
Note 1.4: Ψ_{JT} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtainingθ_{JA}, using a procedure described in JESD51-5.

Marking Information

AD52068

- Marking Information

Line 1：LOGO
Line 2：Product No
Line 3：Tracking Code



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVCC	Supply voltage	PVCCL, PVCCR, AVCC	-0.3	30	V
V_I	Interface pin voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, $\overline{FAULT}$,	-0.3	30	V
		PLIMIT	-0.3	5.5	
T_A	Operating free-air temperature range		-40	85	°C
T_J	Operating junction temperature range		-40	150	°C
T_{stg}	Storage temperature range		-65	150	°C
R_L	Minimum Load Resistance	BTL: PVCC ＞ 13V	4.8		Ω
		BTL: PVCC ≦ 13V	3.2		Ω
		PBTL	3.2		Ω
ESD	Human Body Model			±2k	V
	Charged Device Model			±500	

Recommended Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVCC	Supply voltage	AVCC, PVCCL, PVCCR	4.5	26	V
V_{IH}	High-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL		0.8	V
V_{OL}	Low-level output voltage	FAULT, $R_{PULL-UP}$=100k, V_{CC}=16V		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, V_I=2V, V_{CC}=18V		50	uA
I_{IL}	Low-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, V_I=0.8V, V_{CC}=18V		5	uA
T_A	Operating free-air		-40	85	°C

General Electrical Characteristics

- PVCC=24V, R_L=8Ω, T_A=25°C (unless otherwise noted)

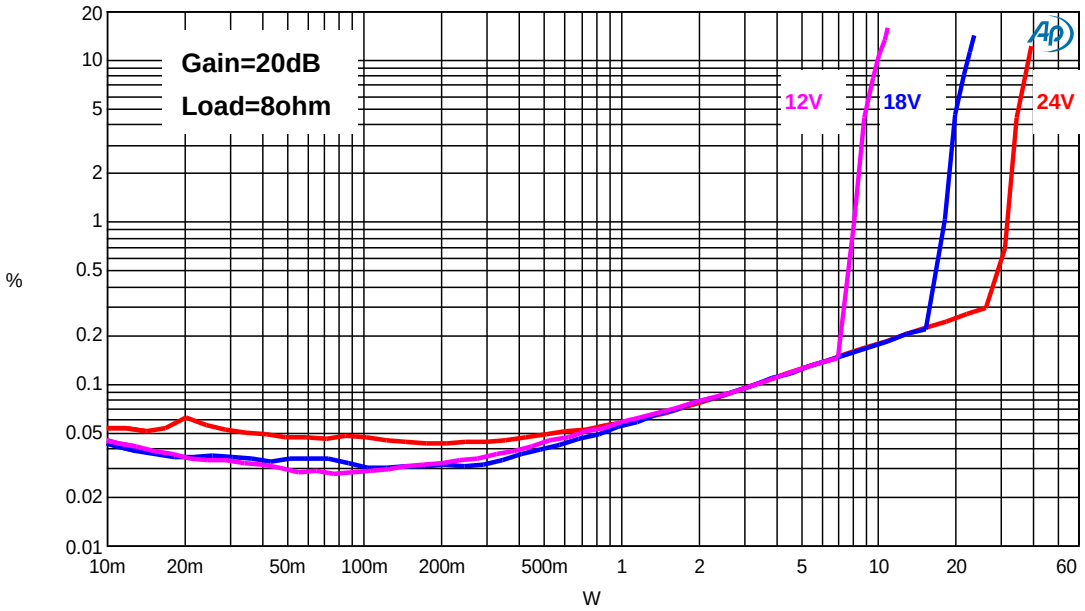
SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
$I_{CC(q)}$	Quiescent supply current	SD=2V, no load, PVCC=12V			20	35	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SD=0.8V, no load, PVCC=12V			< 12	25	uA
$R_{DS(on)}$	Drain-source on-state resistance-High side NMOS	PVCC=12V, Id=500mA, T_J=25 °C			220		mΩ
	Drain-source on-state resistance-Low side NMOS				220		mΩ
$\|V_{OS}\|$	Class-D output offset voltage (measured differential)	PVCC=12V V_I=0V, Gain=36dB			1.5	15	mV
t_{ON}	Turn-on time	SD=2V			90		ms
t_{OFF}	Turn-off time	SD=0.8V			2		us
I_{AVCC}	Operating current for AVCC				8.5	12.8	mA
GVDD	Regulator output	I_{GVDD}=0.1mA		4.75	5	5.25	V
G	Gain	GAIN1 =0.8V	GAIN0=0.8V	19	20	21	dB
			GAIN0=2V	25	26	27	
		GAIN1 =2V	GAIN0=0.8V	31	32	33	
			GAIN0=2V	35	36	37	

Electrical Characteristics and Specifications of Loudspeaker Driver

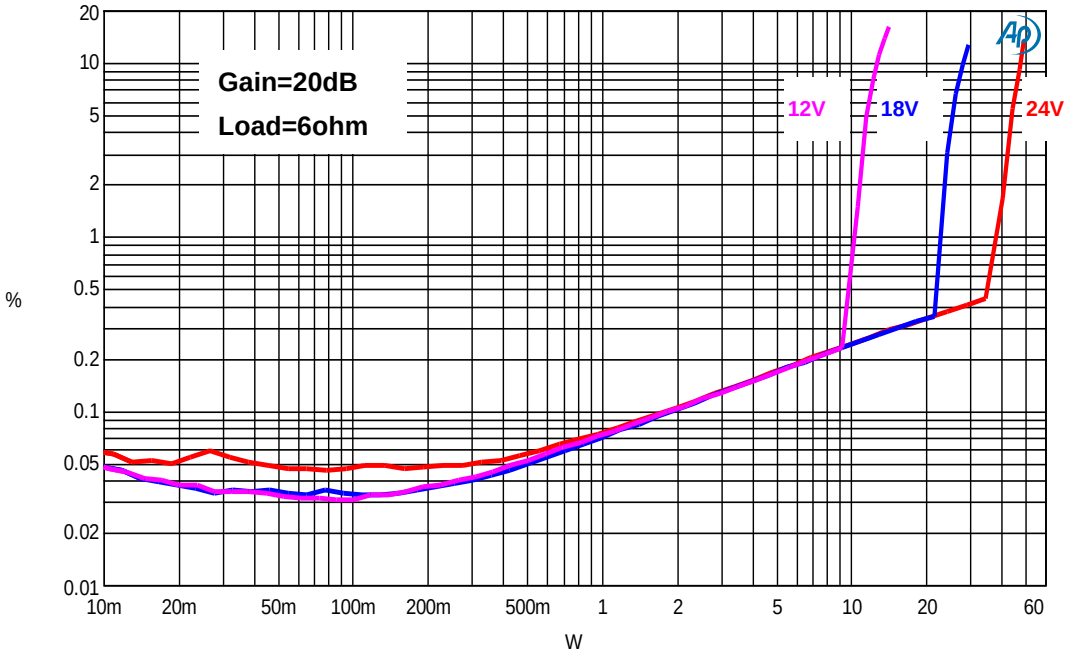
- PVCC=24V, R_L=8Ω with passive LC low-pass filter (L=22uH, C=1uF).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_O	Output power	THD+N=0.28%, f=1kHz, PVCC=24V		20		W
		THD+N=10%, f=1kHz, PVCC=12V		10		
THD+N	Total harmonic distortion plus noise	PVCC=24V, R_L=8Ω, f=1kHz, P_O=10W (half-power)		0.18		%
		PVCC=12V, R_L=8Ω, f=1kHz, P_O=5W (half-power)		0.13		
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=20dB, a-weighted		103		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=20dB, a-weighted filter, R_L=8Ω		93		uV
K_{SVR}	Power Supply Rejection Ratio	V_{ripple}=200mVpp at 1kHz, Gain=20dB, inputs ac-grounded		-70		dB
Crosstalk	Crosstalk	F=1kHz, V_O=1Vrms, Gain=20dB		-90		dB
f_{OSC}	Oscillator frequency		250	310	370	kHz
T_{SENSOR}	Thermal trip point			150		°C
	Thermal hysteresis			25		°C

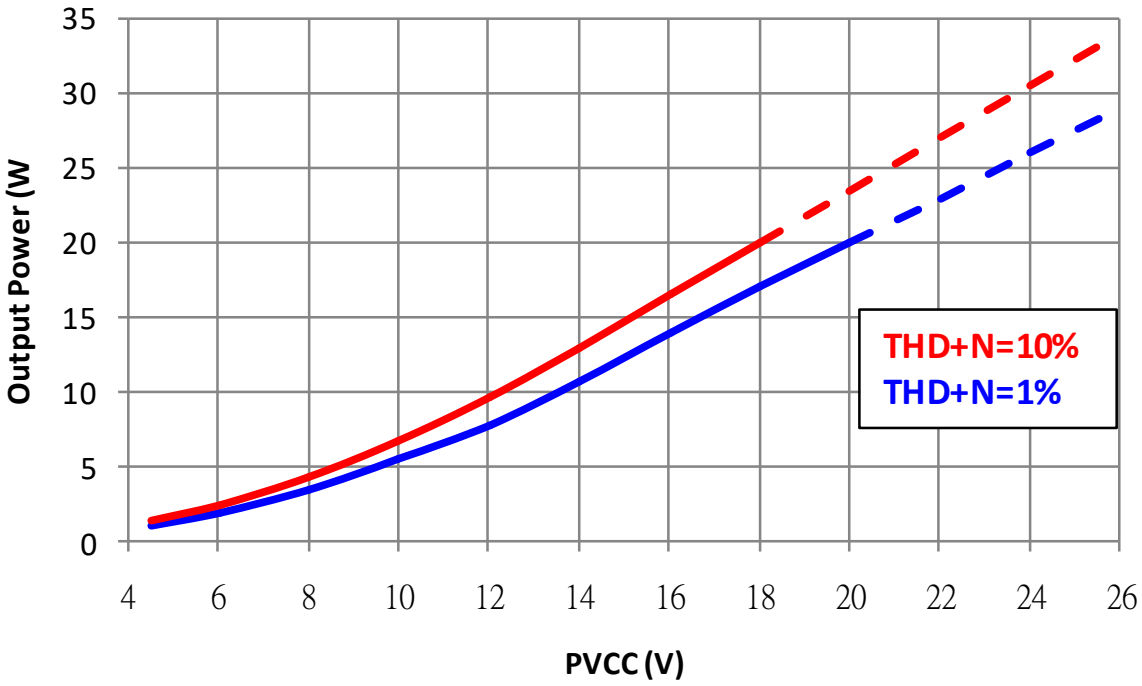
THD + N (%) v.s. Output power (8ohm load)



THD + N (%) v.s. Output power (6ohm load)

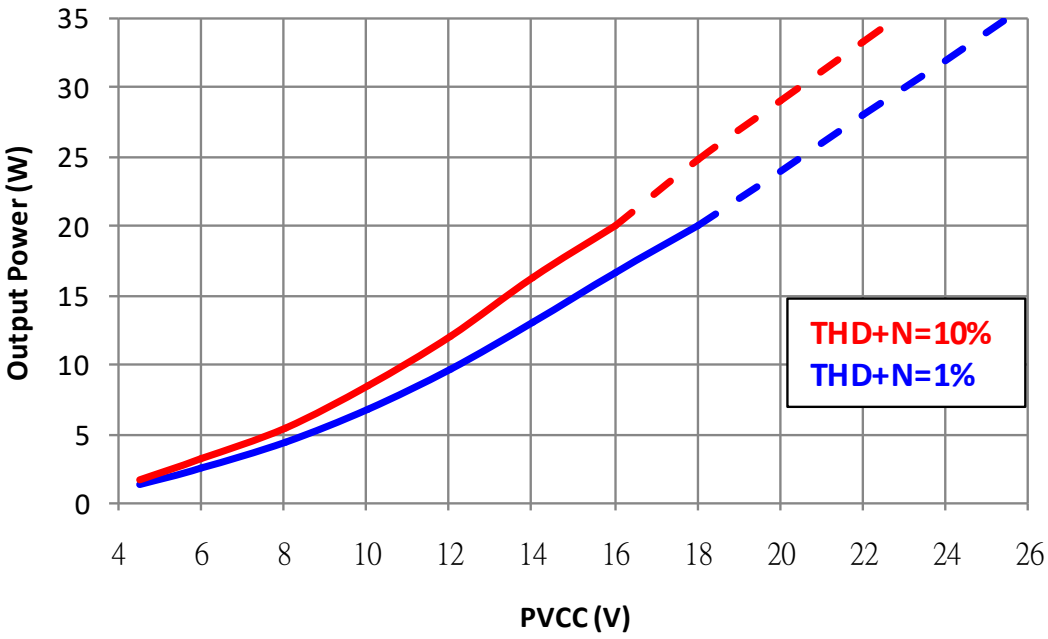


AD52068_8ohm stereo



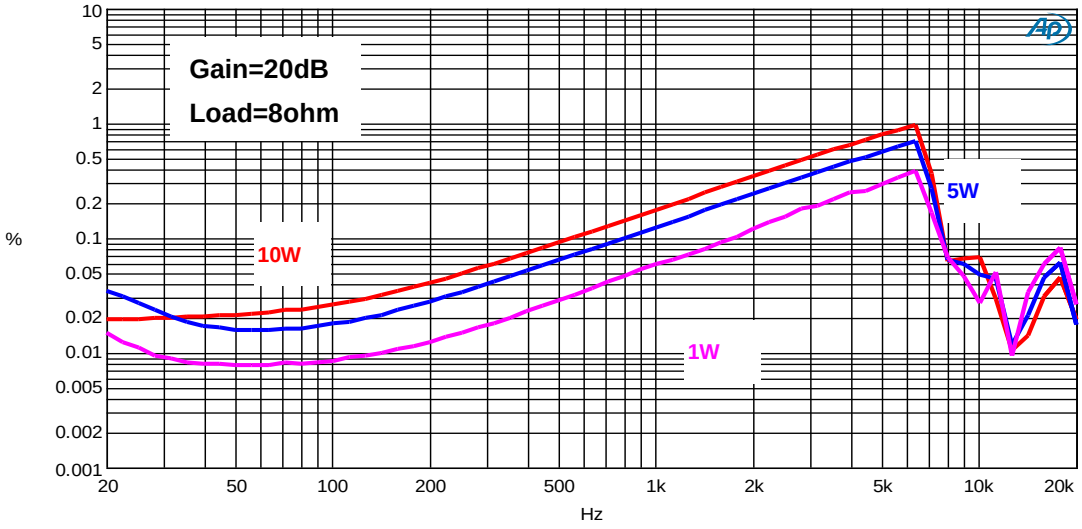
Note: Dashed Line represent thermally limited regions.

AD52068_6ohm stereo

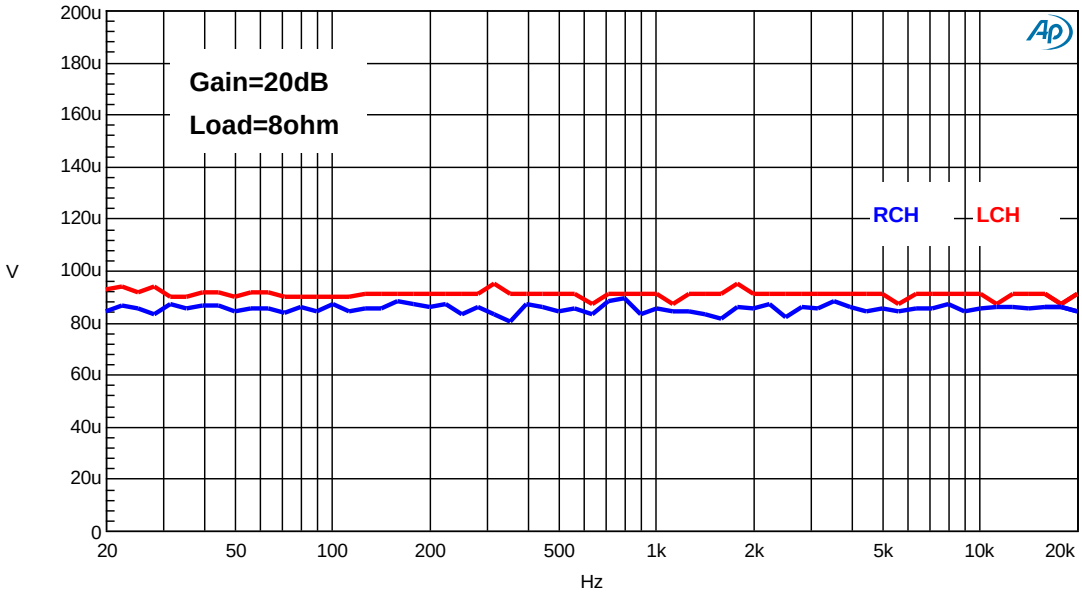


Note: Dashed Line represent thermally limited regions.

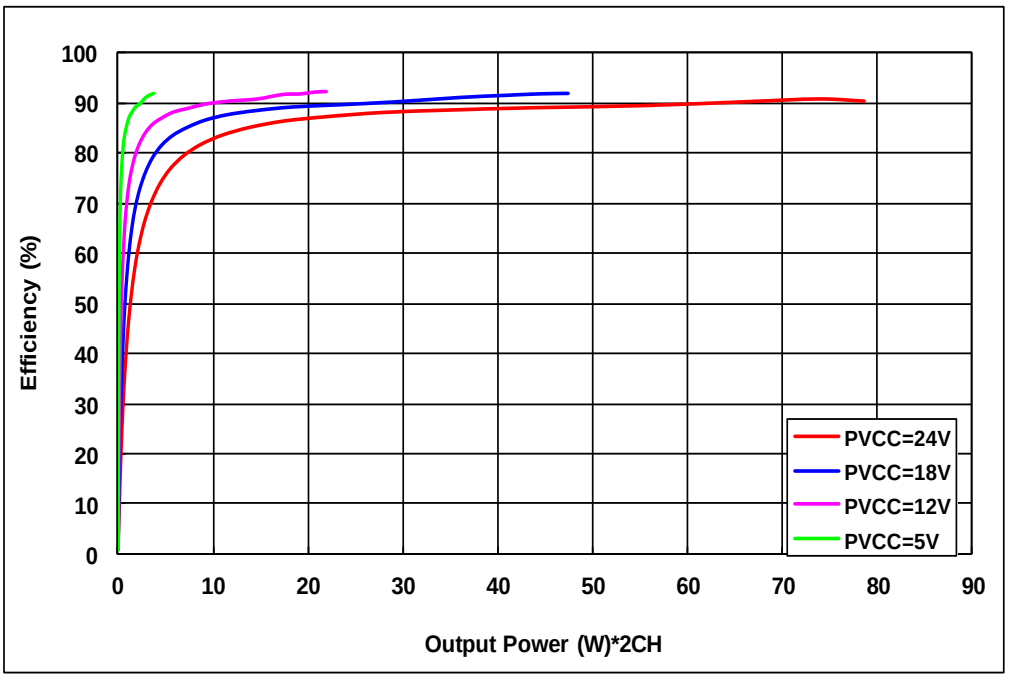
THD + N (%) v.s. Frequency (24V 8ohm load)



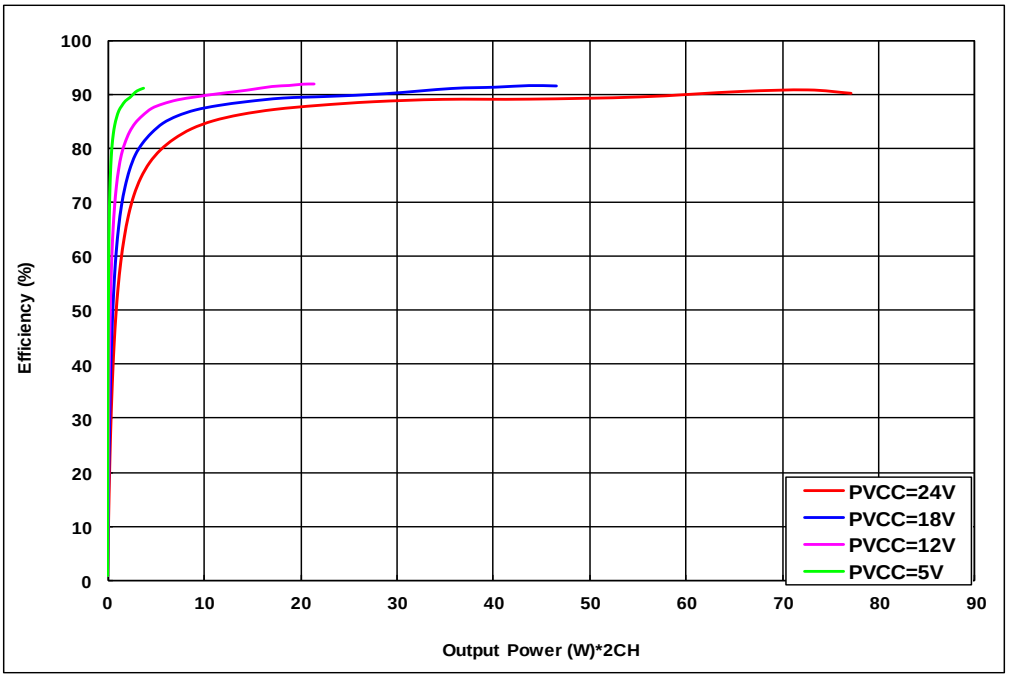
Noise (24V 8ohm load)



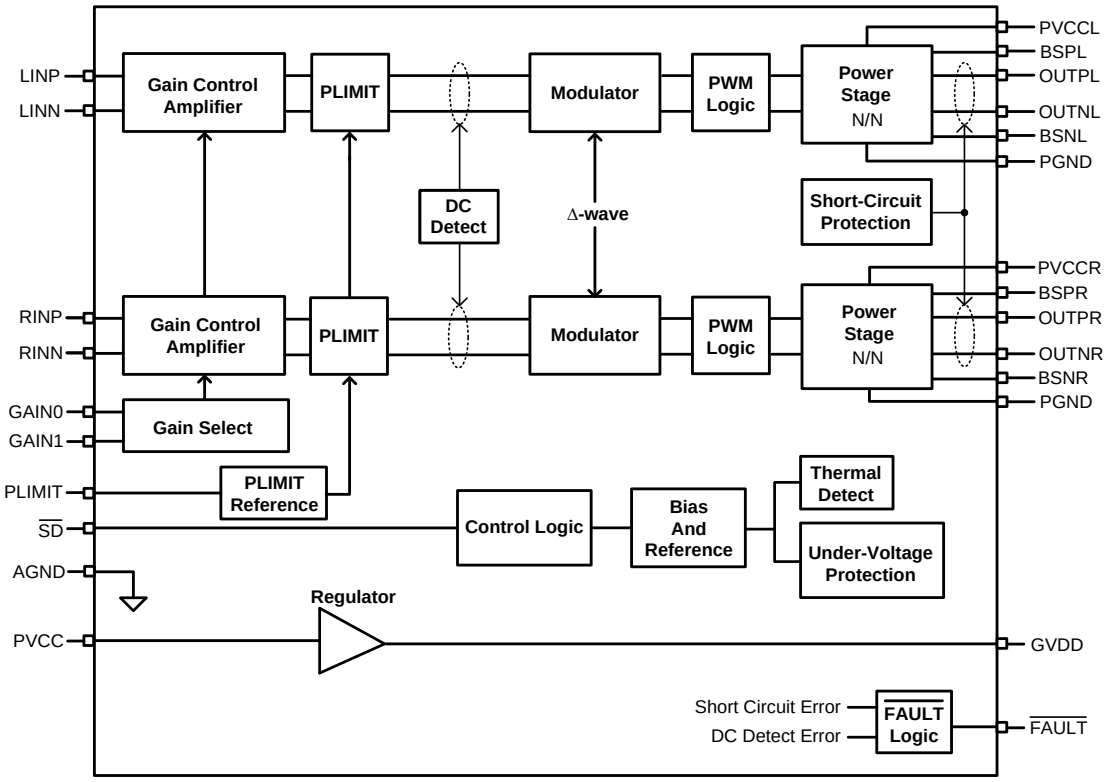
Efficiency (Stereo 8ohm load) / 2ch



Efficiency (Mono 4ohm load)



Functional Block Diagram



Operation Descriptions

- **Gain settings**

  The gain of the AD52068 is set by two input pins, GAIN0 and GAIN1. By varying input resistance in AD52068, the various volume gains are achieved. The respective volume gain and input resistance are listed in Table 1. However, there is 20% variation in input resistance from production variation.

Table 1. Volume gain and input impedance

GAIN1	GAIN0	Volume Gain (dB)	Input Resistance, R_{in} (kΩ)
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

- **Shutdown ($\overline{SD}$) control**

  Pulling $\overline{SD}$ pin low will let AD52068 operate in low-current state for power conservation. The AD52068 outputs will enter mute once $\overline{SD}$ pin is pulled low, and regulator will also disable to save power. If let $\overline{SD}$ pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

- **DC detection**

  AD52068 has dc detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit detects first volume amplifier stage output, when both differential outputs' voltage become higher than a determined voltage or lower than a determined voltage for more than 420ms, the dc detect error will occur and report to $\overline{FAULT}$ pin. At the same time, loudspeaker drivers of right/left channel will disable and enter Hi-Z. This fault can not be cleared by cycling $\overline{SD}$, it is necessary to cycle the PVCC supply.

  The minimum differential input voltages required to trigger the DC detect function are shown in table2. The input voltage must keep above the voltage listed in the table for more than 420msec to trigger the DC detect fault. The equivalent class-D output duty of the DC detect threshold is listed in table3.

Table 2. DC Detect Threshold

AV (dB)	Vin (mV, differential)
20	250
26	125
32	63
36	35

Table 3. Output DC Detect Duty (for Either Channel)

PVCC (V)	Output Duty Exceeds
8	20.8%
12	20.8%
16	20.8%

- **Thermal protection**

  If the internal junction temperature is higher than 150°C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature for AD52068 returning to normal operation is about 125°C. The variation of protected temperature is about 10%. Thermal protection faults are NOT reported on the $\overline{\text{FAULT}}$ pin.

- **Short-circuit protection**

  To protect loudspeaker drivers from over-current damage, AD52068 has built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other or shorted to VSS or to PVCC, overload detectors may activate. Once one of right and left channel overload detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The short protection fault is reported on $\overline{\text{FAULT}}$ pin as a low state. The latch can be cleared by reset $\overline{\text{SD}}$ or power supply cycling.

  The short circuit protection latch can have auto-recovery function by connect the $\overline{\text{FAULT}}$ pin directly to $\overline{\text{SD}}$ pin. The latch state will be released after 420msec, and the short protection latch will re-cycle if output overload is detected again.

- **Under-voltage detection**

  When the GVDD voltage is lower than 2.8V or the AVCC voltage is lower than 4V, loudspeaker drivers of right/left channel will be disabled and kept at low state. Otherwise, AD52068 return to normal operation.

- **Over-voltage protection**

  When the AVCC voltage is higher than 29.5V, loudspeaker will be disabled kept at low state. The protection status will be released as AVCC lower than 29V.

- **Power limit function**

  - The voltage at PLIMIT pin can used to limit the power of first gain control amplifier output. Add a resistor divider from GVDD to ground to set the voltage V_{PLIMIT} at the PLIMIT pin. The voltage V_{PLIMIT} sets a limit on the output peak-to-peak voltage. PLIMIT is adjustable from 1.33V~2.5V. If the output power >20W in stereo (or >40W in mono), the power limit setting disable is prohibited.

For normal BTL operation (Stereo) and PBTL (Mono) operation:

$$Po@1\% = \frac{\left[\frac{2.5V - V_{PLIMIT}}{2.1V + 0.81 \times V_{PLIMIT}} \times 2 \times PVDD \times (1.22 - 0.0092 \times PVDD)\right]^2}{2 \times R_L}$$

$$Po@10\% = (Po@1\%) \times (1.21 + 0.021 \times PVDD)$$

Connect PLIMIT pin to ground or GVDD to disable power limit function. The output variation during power limit feature enable may have +-20% variation due to process window.

Table 4. PLIMIT Typical Operation Ⅰ

Test Conditions	Output P_O (W)	V_{PLIMIT} (V) @ THD+N=10%
PVCC=24V RL=8Ω	5	1.954
	8	1.835
	10	1.779
	12	1.731
	15	1.67

Table 4.1 PLIMIT Typical Operation Ⅱ

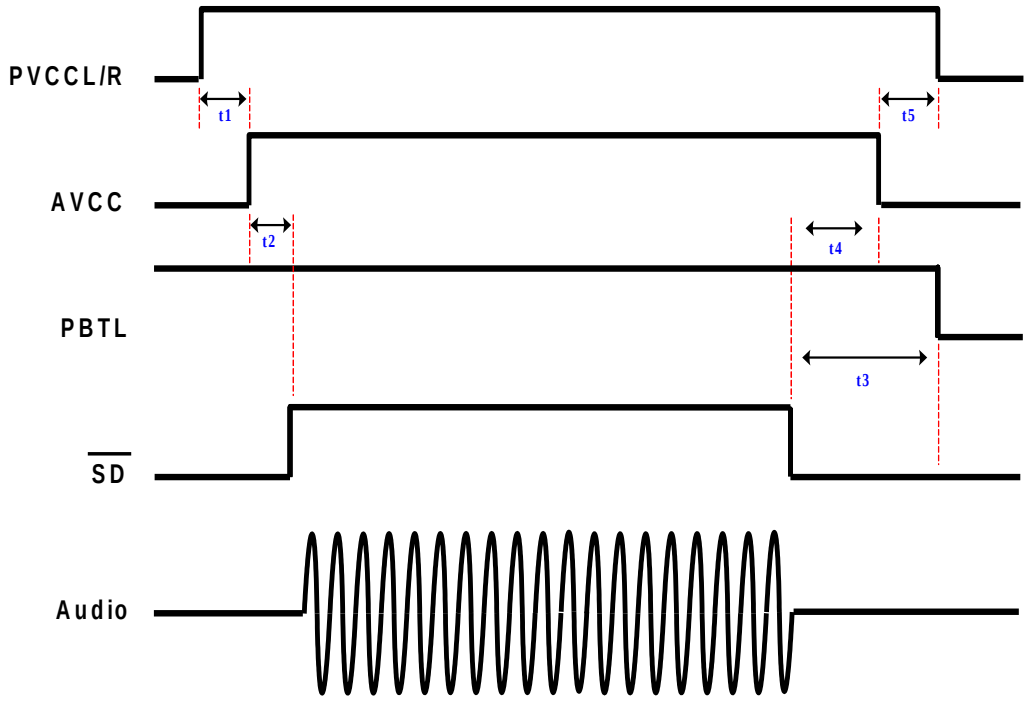
Test Conditions	Output P_O (W)	V_{PLIMIT} (V) @ THD+N=10%
PVCC=12V RL=8Ω	3	1.756
	5	1.584
	8	1.37
	9	1.283

- **PBTL (Mono) function**

  AD52068 provides the application of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin is tied high, the positive and negative outputs of left and right channel are synchronized and in phase. Apply the input signal to the RIGHT channel input in PBTL mode and let the LEFT channel input grounded, and place the speaker between the LEFT and RIGHT outputs. The output swing is doubled of that in normal mode. See the application circuit example for PBTL (Mono) mode operation. For normal BTL (Stereo) operation, connect the PBTL pin to ground.

- **Power On/Off sequence**

  Hereunder is AD52068's power on/off sequence.



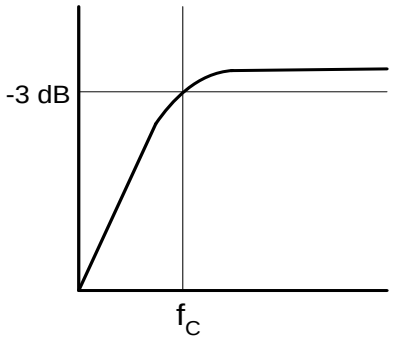
Symbol	Min. (ms)	Typ. (ms)	Max. (ms)
t1	0	-	-
t2	0.1	-	-
t3	0.2 (Don't care for PBTL=0 in stereo operating)	-	-
t4	0.1	-	-
t5	0	-	-

Application information

- **Input capacitors (C_{in})**

  The performance at low frequency (bass) is affected by the corner frequency (f_c) of the high-pass filter composed of input resistor (R_{in}) and input capacitor (C_{in}), determined in equation (2). Typically, a 0.1μF or 1μF ceramic capacitor is suggested for C_{in}. The resistance of input resistors is different at different gain setting. The respective gain and input resistance are listed in Table 1 (shown at GAIN SETTING). However, there is 20% variation in input resistance from production variation.

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \ (\text{Hz}) \quad \cdots\cdots\cdots (2)$$



- **Ferrite Bead selection**

  If the traces from the AD52068 to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.

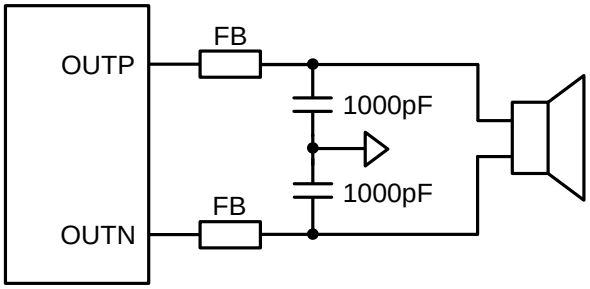


Figure 2. Typical Ferrite Bead Filter

- **Output LC Filter**

  If the traces from the AD52068 to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Figure 3 shows the typical output filter for 8Ω speaker with a cut-off frequency of 33 kHz and Figure 4 shows the typical output filter for 4Ω speaker with a cut-off frequency of 33 kHz.

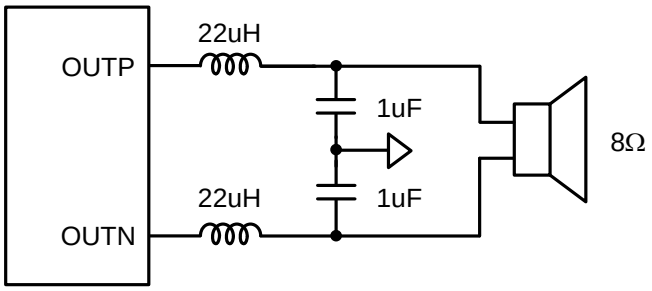


Figure 3. Typical LC Output Filter for 8Ω Speaker

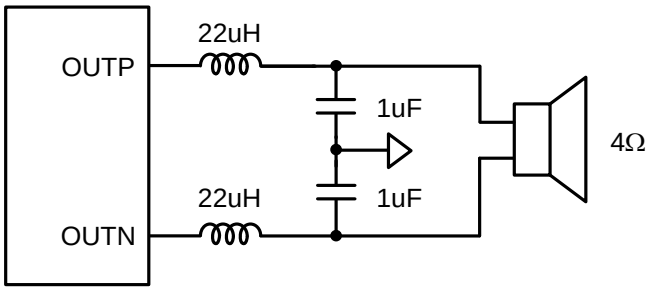


Figure 4. Typical LC Output Filter for 4Ω Speaker

- **Power supply decoupling capacitor (Cs)**

  Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVCC and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1μF or 1μF as close as possible to the device PVCC leads works best. For low frequency noise filtering, a 100μF or greater capacitor (tantalum or electrolytic type) is suggested.

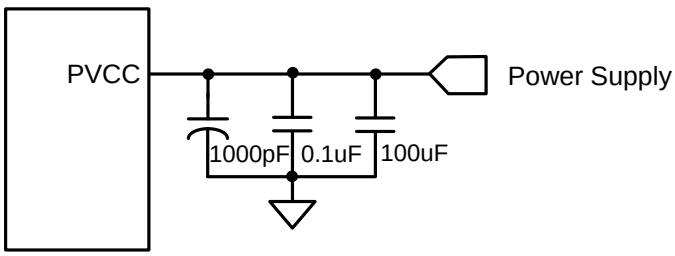
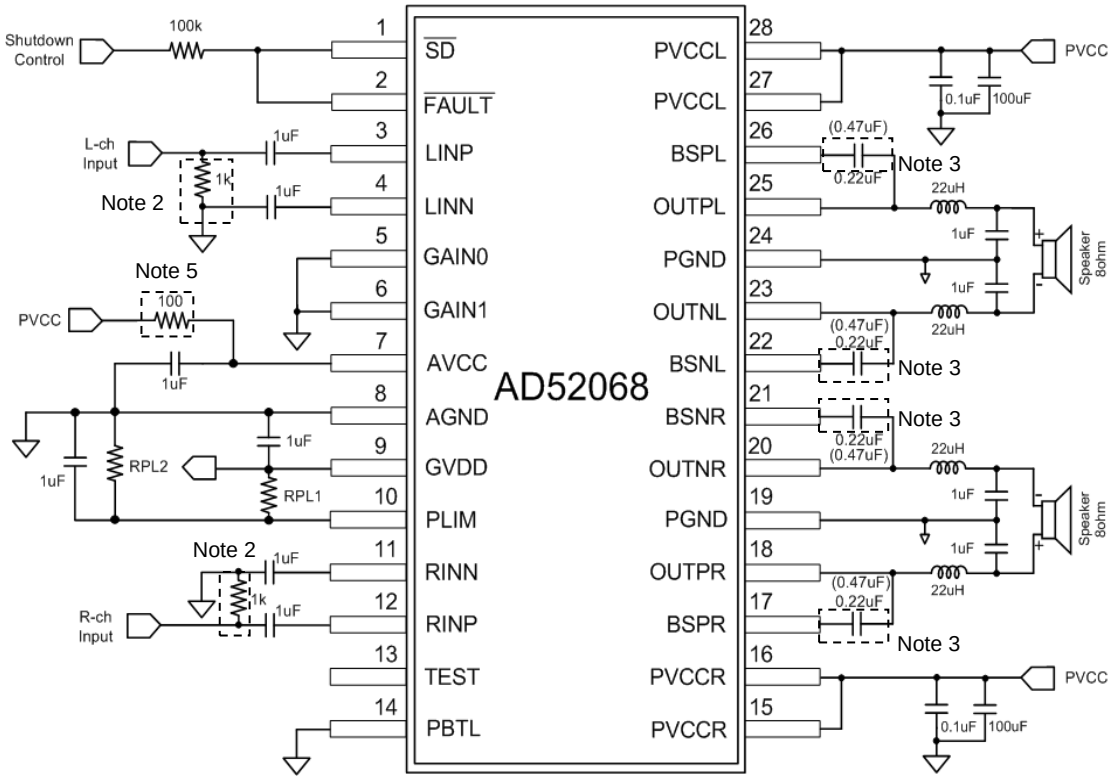


Figure 5. Recommended Power Supply Decoupling Capacitors.

Application Circuit Example

- Application circuit for BTL (Stereo) mode configuration and Singe-Ended Input



Note 2: These resistances must be connected to ground, resistance=1Kohm.

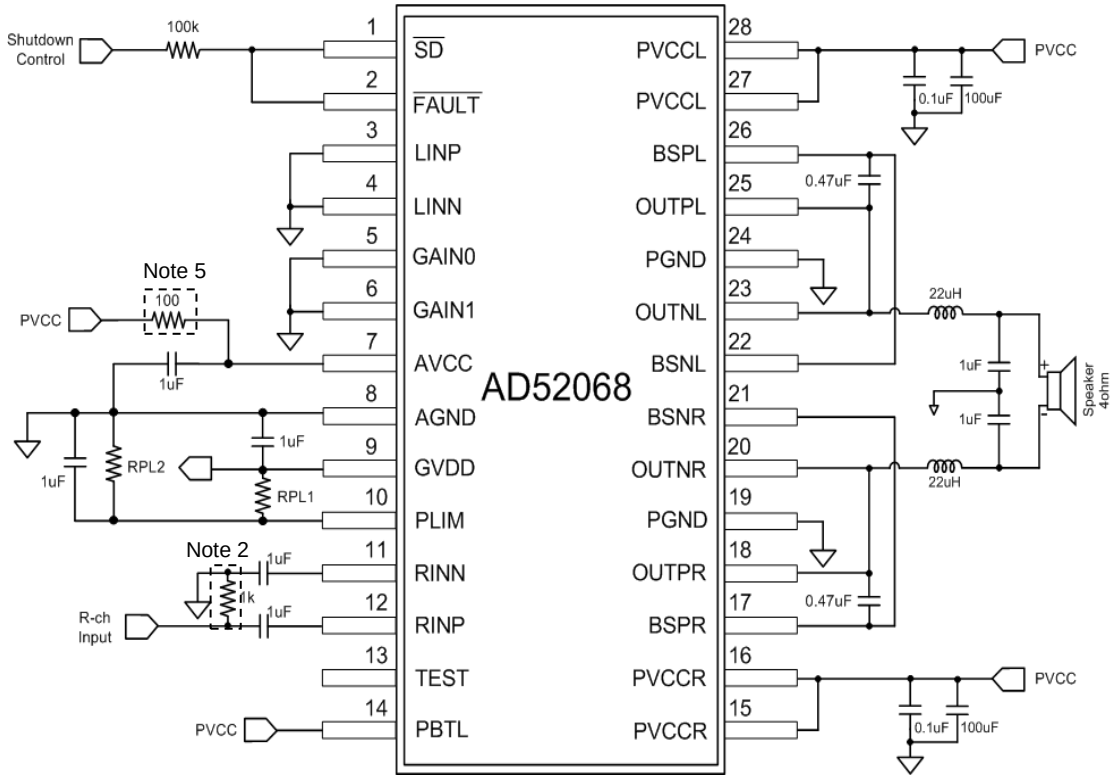
Note 3: These capacitors should be change to 0.47uF, while the PVCC<=5V.

Note 5: The under-voltage threshold for AVCC could be adjusted by R_{AVCC}, the formula will be followed

$$R_{AVCC} \le \frac{PVCC-4}{30}(k\Omega)$$ ***to adjust it..***

Application Circuit Example

- Application circuit for parallel BTL (Mono) mode configuration and Singe-Ended Input



Note 2: These resistances must be connected to ground, resistance=1Kohm.

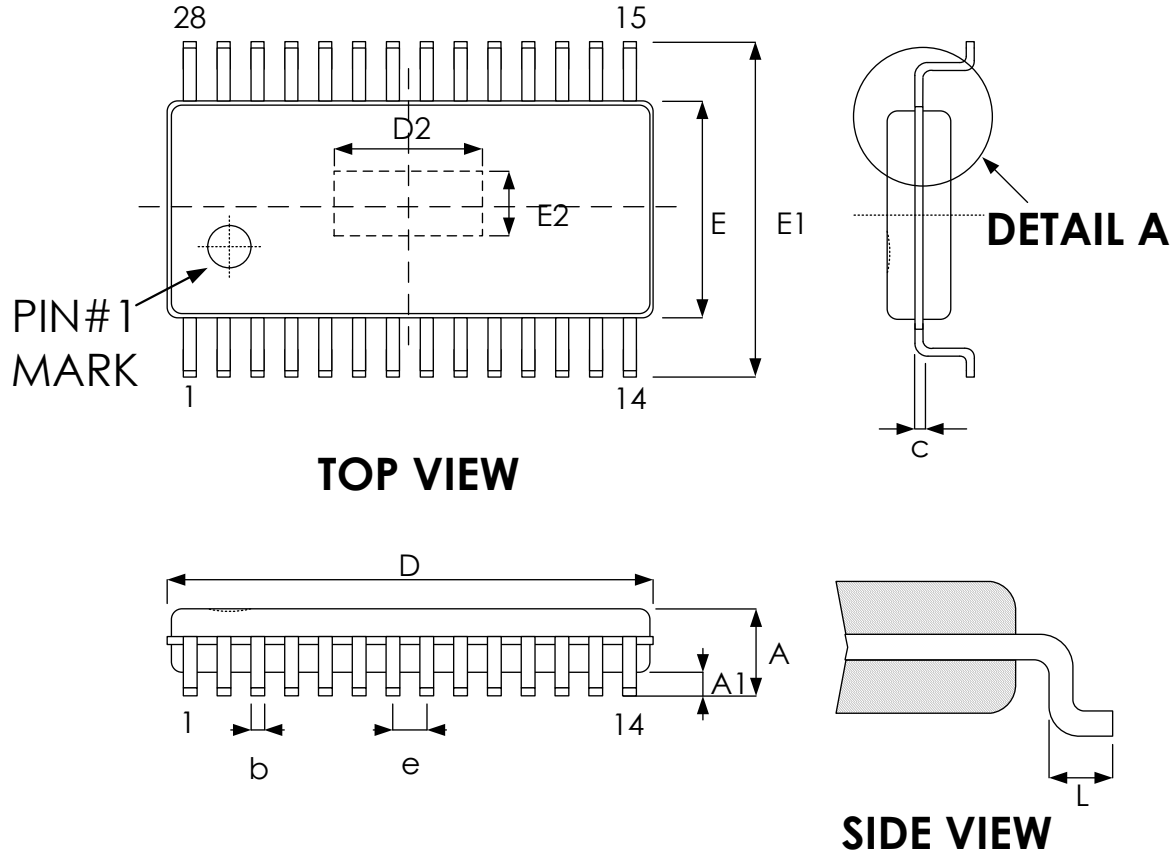
Note 4: Be noted that input should be applied on R-channel only for Mono application.

Note 5: The under-voltage threshold for AVCC could be adjusted by R_{AVCC}, the formula will be followed

$$R_{AVCC} \le \frac{PVCC-4}{30}(k\Omega)$$ ***to adjust it.***

Package Dimensions

TSSOP-28 (173 mil)



Symbol	Dimension in mm	
	Min	Max
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	3.40	6.40
E2	2.50	2.90

Revision History

Revision	Date	Description
0.1	2016.09.29	Initial version.
1.0	2016.11.15	Modified version to 1.0, removed preliminary
1.1	2016.11.09	Modified Package Dimensions
1.2	2017.03.16	1) Modify performance data with LC filter. 2) Modify application circuit with LC filter.
1.3	2017.04.19	1) Added performance data. 2) Modified Absolute maximum ratings. Page.4, 7, 8
1.4	2018.01.22	Modify ESD data.
1.5	2018.06.11	Modify MOQ for AD52068-QG28NRR
1.6	2019.01.21	1) Modify application circuit(stereo & Mono). 2) Modify gain electrical characteristics. 3) Modify Package dimension.
1.7	2019.03.21	Remove AD52068-QG28NRT for order information
1.8	2020.01.09	Update operation descriptions for under-voltage detection. Update application circuit.
1.9	2020.01.17	Modify pin description.
2.0	2020.02.03	Modify power limit function.
2.1	2020.07.16	Update Package Dimensions “D2”
2.2	2021.04.27	Modify power limit formula.
2.3	2021.05.20	Modify pin description.
2.4	2021.10.28	1) Added I_{AVCC} spec. into. 2) Modified OVP description. 3) Updated R_{AVCC} formula in application circuit. 4) Added power on/off sequence into.

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