SGM4703

High-Power Stereo Class-D Audio Power Amplifier with Adjustable Power Limit and Automatic Level Control

GENERAL DESCRIPTION

The SGM4703 is a high-power, high efficiency, stereo Class-D audio power amplifier with adjustable power limit (APL) and automatic level control (ALC). It operates with a wide range of supply voltages from 5V to 26V. With 24V supply voltage, it can deliver 2 × 40W peak output power for a pair of 8Ω speakers with 10% THD+N.

The high efficiency of SGM4703 extends battery life in playing music and allows it to deliver an output power of 2 × 20W without the need for a bulky heat sink on a two-layer system board. Its high PSRR and low EMI emission reduce system design and manufacturing complexities, as well as lower system cost.

The SGM4703 features APL and ALC. The APL limits peak audio outputs to a user-defined value to protect audio speakers from excessive power dissipation or over-load. The APL and ALC adjust the voltage gain of the audio amplifiers in response to over-limit audio inputs, eliminating output clipping distortion while maintaining a maximally allowed dynamic range of audio outputs. The limiting voltage of APL and ALC can be either a user-defined value or the supply voltage.

The SGM4703 can be configured into driving either a pair of speakers in Bridge-Tied-Load (BTL) configuration for stereo applications or a single speaker in Parallel BTL (PBTL) configuration for mono applications.

The SGM4703 features two PWM modulation schemes for Class-D audio amplifiers: Dual-Side-Modulation (DSM) and Single-Side-Modulation (SSM).

In SGM4703, comprehensive protection modes against various operating faults ensure its safe and reliable operation.

FEATURES

- **Wide Range of Supply Voltages from 5V to 26V**
- **Adjustable Power Limit to Safeguard Audio Speakers**
- **Automatic Level Control to Eliminate Output Clipping**
- **4 Selectable Gain Settings: 20/26/30/34dB**
- **3 Selectable ALC Dynamic Characteristics**
- **2 Selectable PWM Frequencies with Optional Spread-Spectrum: 360kHz and 500kHz**
- **2 Selectable Modulation Schemes: SSM and DSM**
- **Optional PBTL Configuration for Mono Applications**
- **Maximum Output Power in Non-ALC**
  - **2 × 40W (V_{DD} = 24V, 8Ω + 33μH, BTL, THD+N = 10%)**
  - **2 × 32W (V_{DD} = 24V, 8Ω + 33μH, BTL, THD+N = 1%)**
  - **80W (V_{DD} = 24V, 4Ω + 33μH, PBTL, THD+N = 10%)**
  - **64W (V_{DD} = 24V, 4Ω + 33μH, PBTL, THD+N = 1%)**
- **ALC Output Power (THD+N < 0.5%) in ALC**
  - **2 × 30W (V_{DD} = 24V, 8Ω + 33μH, BTL)**
  - **2 × 21W (V_{DD} = 15V, 4Ω + 33μH, BTL)**
  - **60W (V_{DD} = 24V, 4Ω + 33μH, PBTL)**
- **Wide ALC Dynamic Range: 12dB (V_{DD} = 12V)**
- **Low THD+N: 0.02% (V_{DD} = 12V, 4Ω + 33μH, P_O = 10W/CH)**
- **High PSRR: 80dB at 1kHz with SSM**
- **Protection Modes against Various Operating Faults Including Under-Voltage, Over-Voltage, Over-Current, Over-Temperature and DC-Detect**
- **Available in a Green TSSOP-28 (Exposed Pad) Package**

APPLICATIONS

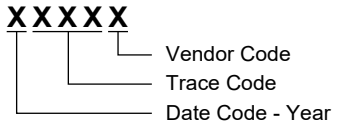
Bluetooth/Wireless Speakers
Consumer Audio Speakers
Soundbars

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM4703	TSSOP-28 (Exposed Pad)	-40℃ to +85℃	SGM4703YPTS28G/TR	SGM4703 YPTS28 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Pins
AVDD, PVDD ..... -0.3V to 30V
Digital I/O Pins
EN, FAULTB ..... -0.3V to V_{AVDD} + 0.3V
MODS ..... -0.3V to V_{GVDD} + 0.3V
Analog Output Pins
GVDD ..... -0.3V to 6.5V
ALC, GAIN, FREQ ..... -0.3V to V_{GVDD} + 0.3V
Analog Input Pins
INPL/R, INNL/R, PLIMIT ..... -0.3V to V_{GVDD} + 0.3V
Package Thermal Resistance
TSSOP-28 (Exposed Pad), θ_{JA} ..... 28℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 1500V
CDM 1000V

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range (1, 2)	V_{DD}	PVDD, AVDD	5		26	V
Operating Ambient Temperature	T_A		-40		+85	℃
Minimum Load Impedance (3)	R_L	BTL Configuration (Stereo)		4		Ω
		PBTL Configuration (Mono)		3		
Audio Input Capacitor	C_{IN}	At INPL/R, INNL/R		1		μF
Maximum Audio Input Voltage Level	$V_{IN, MAX}$	At INNL/R, INPL/R			2.0	V_{RMS}
PLIMIT Voltage Range	V_{PLIMIT}	PLIMIT	0		V_{GVDD}	V
Maximum Load Current at GVDD	I_{LOAD}				5	mA
Supply Decoupling Capacitor	C_{PVDD}	Ceramic		1		μF
		Electrolytic or Tantalum (4)		220		
	C_{AVDD}	Ceramic		1		
	C_{GVDD}	Ceramic		1		
	C_{PLIMIT}	Ceramic		0.1		
Bootstrap Holding Capacitor	C_B	At BSTPL/R, BSTNL/R		0.1		μF
Mono Mode Select	INNR INPR	PBTL Configuration	Both Pins Shorted to GND			
Modulation Scheme Select	MODS	Single-Side-Modulation (SSM)	High or Open			
		Double-Side-Modulation (DSM)	Low			
Voltage Gain Select	GAIN	26dB	Open			
		30dB	Shorted to GND			
		34dB	68kΩ to GND			
		20dB	300kΩ to GND			
ALC Mode Select	ALC	Non-ALC	Open			
		ALC-1	Shorted to GND			
		ALC-2	68kΩ to GND			
		ALC-3	300kΩ to GND			
PWM Frequency Select	FREQ	Constant Frequency at 360kHz	Open			
		360kHz with Spread-Spectrum	Shorted to GND			
		Constant Frequency at 500kHz	68kΩ to GND			
		500kHz with Spread-Spectrum	300kΩ to GND			

NOTES:

1. The peak supply voltage including its tolerance over various operating conditions must not exceed its absolute-maximum-rated value (26V). Exposure to absolute-maximum-rated supply voltage may damage the device or affect device reliability permantly.

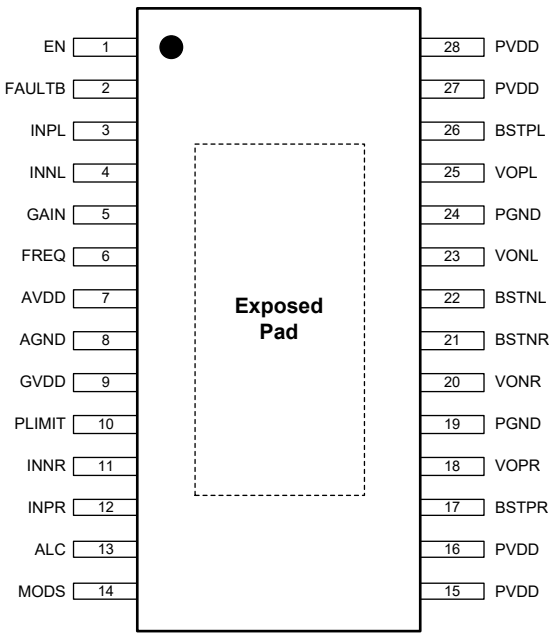
2. For high power applications, the maximum power supply V_{DD} that can be applied to the SGM4703 is largely limited by the thermal dissipation capability of the package and the system board layout.

3. The SGM4703 is specfied with an 8Ω resistive load in series with 33μH inductive load or with a 4Ω resistive load in series with 33μH inductive load or with a 2Ω or 3Ω resistive load in series with 15μH inductive load (in PBTL configuration). Without inductive loads, the maximum continous output power will severely suffer from efficiency and thermal degradation.

4. If the input supply is located more than a few centimeters from SGM4703, additional bulk capacitor may be required in addition to the ceramic capacitors.

PIN CONFIGURATION

(TOP VIEW)



TSSOP-28 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	EN	DI	Chip enable (active high) with an on-chip 250kΩ pull-down resistor to ground. A TTL logic input in compliance with AVDD.
2	FAULTB	DO	Open-drain output indicating operational faults of OCP or DCP. Both faults can be set for auto-recovery by externally connecting FAULTB to EN. Otherwise, both OCP and DCP faults must be reset by cycling EN.
3	INPL	AI	Left-channel non-inverting audio input biased at one half of GVDD.
4	INNL	AI	Left-channel inverting audio input biased at one half of GVDD.
5	GAIN	AO	Voltage gain select with an on-chip 250kΩ pull-down resistor to ground. Connect to a resistor to ground to set the voltage gain of the audio amplifiers.
6	FREQ	AO	PWM frequency select with an on-chip 250kΩ pull-down resistor to ground. Connect to a resistor to ground to set the PWM frequency with optional spread-spectrum.
7	AVDD	P	Analog supply. Connect to a 1μF capacitor for decoupling. Also, add a decoupling resistor of 10Ω between this pin and the system power supply for high-frequency filtering.
8	AGND	G	Analog ground. Connect to the system power ground GND.
9	GVDD	AO	Internally generated reference voltage at 5.6V. Connect to a 1μF capacitor for decoupling.
10	PLIMIT	AI	Adjustable power limit. Connect to a resistor divider from GVDD to AGND to set the output voltage limit. Add a 0.1μF capacitor for decoupling.
11	INNR	AI	Right-channel inverting audio input biased at one half of GVDD. Connect to ground (without decoupling capacitor) for mono mode in PBTL configuration.
12	INPR	AI	Right-channel non-inverting audio input biased at one half of GVDD. Connect to ground (without decoupling capacitor) for mono mode in PBTL configuration.
13	ALC	AO	ALC mode select with an on-chip 250kΩ pull-down resistor to ground. Connect to a resistor to ground or leave open to set ALC dynamic characteristic.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	DESCRIPTION
14	MODS	DI	PWM modulation select with an on-chip 250kΩ pull-up resistor to GVDD. A TTL logic input in compliance with GVDD.
15, 16	PVDD	P	Power supply inputs for the right-channel H-bridge. The power supplies for right-channel and left-channel H-bridges are internally.
17	BSTPR	AO	Connect to bootstrap holding capacitor for the right-channel non-inverting output, VOPR. A 0.1μF capacitor must be placed between this pin and VOPR for proper operation.
18	VOPR	AO	Right-channel non-inverting audio output terminal.
19	PGND	G	Power ground for the right-channel H-bridge. Connect to the system ground GND. The power ground for right-channel and left-channel H-bridges are internally shorted.
20	VONR	AO	Right-channel inverting audio output terminal.
21	BSTNR	AO	Connect to a bootstrap holding capacitor for the right-channel inverting output, VONR. A 0.1μF capacitor must be placed between this pin and VONR for proper operation.
22	BSTNL	AO	Connect to a bootstrap holding capacitor for the left-channel inverting output, VONL. A 0.1μF capacitor must be placed between this pin and VONL for proper operation.
23	VONL	AO	Left-channel inverting audio output terminal.
24	PGND	G	Power ground for the left-channel H-bridge. Connect to the system ground GND. The power ground for right-channel and left-channel H-bridges are internally shorted.
25	VOPL	AO	Left-channel non-inverting audio output terminal.
26	BSTPL	AO	Connect to a bootstrap holding capacitor for the left-channel non-inverting output, VOPL. A 0.1μF capacitor must be placed between this pin and VOPL for proper operation.
27, 28	PVDD	P	Power supply inputs for the left-channel H-bridge. The power supplies for right-channel and left-channel H-bridges are internally shorted.
Exposed Pad	GND	G	Exposed pad. Connect to the system ground GND.

TYPICAL APPLICATION

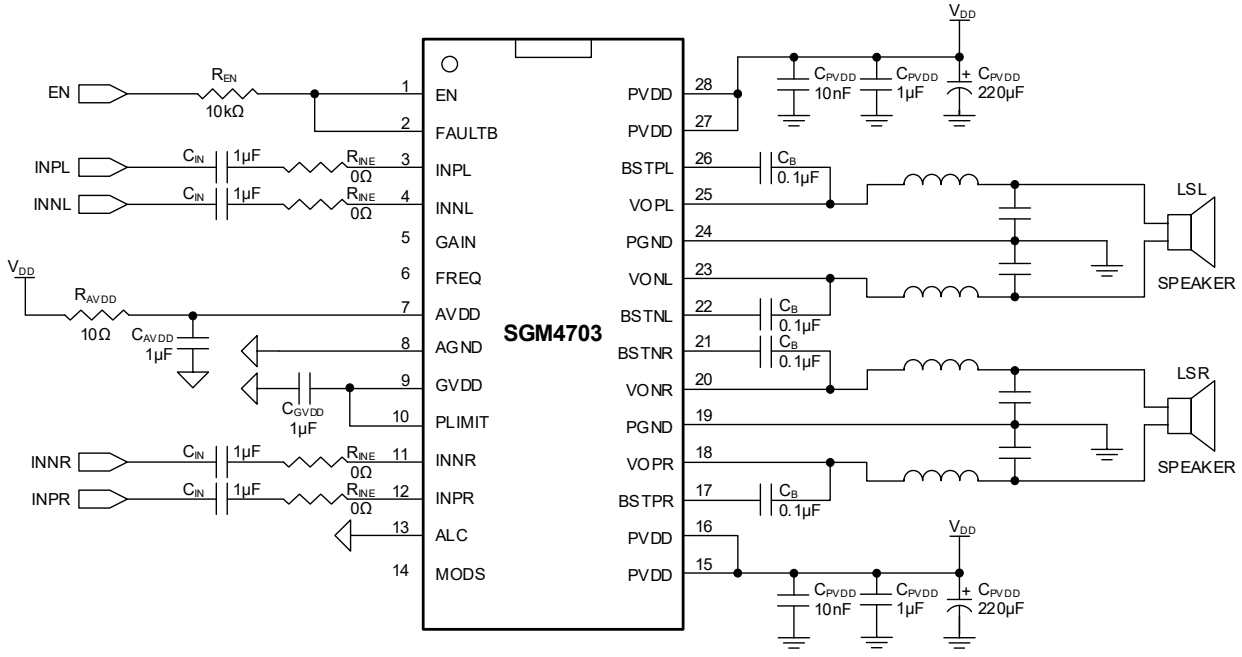


Figure 1. Typical Application Circuit

IMPORTANT APPLICATION NOTES

Output Power Considerations

1. The maximum output power of SGM4703 is determined primarily by the power supply (its output voltage and current) and speaker impedance. As a high power audio amplifier, the maximum output power of SGM4703 can be severely limited by the thermal dissipation capability of the system board layout.

2. The SGM4703 is packaged with an exposed thermal pad on the underside of the device. Solder the thermal pad directly onto a large grounded metal island (GND) underneath the package, as a thermal sink for proper thermal dissipation. On the grounded metal island, place several rows of solid, equally-spaced vias connecting to the bottom layer of the system board. Failure to do so can severely limit its thermal dissipation capability. It might even cause the device going into over-temperature mute occasionally.

3. Use wide open areas around the SGM4703 on the top and bottom layers of the system board as the ground plane GND. Place lots of solid vias connecting the top and bottom layers of GND. Furthermore, for proper thermal dissipation, reserve wide and uninterrupted GND areas along the thermal flow on the top layer, i.e., no wires cutting through the GND layer and obstructing the thermal flow in the proximity of the device.

4. All the power ground pins PGND are directly shorted to the ground plane GND as a central “star” ground for the SGM4703. Use a single point of connection between the analog ground AGND and the ground plane GND to minimize the coupling of high-current switching noise onto audio signals.

5. The power supply pins, PVDD, for the audio amplifiers’ output stages are directly connected together with short and wide metal traces.

6. Use direct and low-impedance traces from the audio outputs (VOPL/R and VONL/R) to their individual output filters and speakers.

Output Filter Considerations

7. For most applications, the SGM4703 does not require an LC output filter when speaker wires are less than 10cm.

8. A ferrite bead filter constructed from a ferrite bead and a ceramic capacitor can be used to suppress EMI. Choose a ferrite bead with a rated current no less than 4A for 8Ω loads, 7A for 4Ω loads, and 9A for 3Ω or less loads (in PBTL configuration). Place the filter tightly together and as close as possible to the audio amplifier’s output pins. A ferrite bead filter can also reduce high-frequency interference.

9. For applications where EMC requirements are extremely stringent or speaker wires are long, use a second-order LC low-pass filter. Place the filter tightly together and as close as possible to the audio amplifier’s output pins. The LC output filter must be designed specifically for the speaker load since the load impedance affects the quality factor of the filter.

General Considerations

10. The SGM4703 requires adequate power supply decoupling to ensure its peak output power, high efficiency, low distortion, and low EMI emissions. Place each supply decoupling capacitor as individually close as possible to AVDD and PVDD pins.

11. Place a small decoupling resistor (10Ω) between the system power supply and AVDD to prevent high frequency Class-D transient spikes from interfering with the on-chip linear amplifiers.

12. For best noise performance, use differential inputs from the audio source for SGM4703. In single-ended input applications, the unused inputs of SGM4703 must be AC-grounded at the audio source. Also, take care to match the impedances seen at two differential inputs closely.

13. The maximum input signal dictates the required voltage gain to achieve the desired maximum output power. For best noise performance, consider a voltage gain as low as possible.

14. Do not alter the logic state of the MODS pin while the device is in operation. To change the setting of the pin, the device must be first brought into shutdown mode by pulling the EN pin low for at least 10ms before it can be restored to its normal operation.

TEST SETUP FOR ELECTRICAL AND PERFORMANCE CHARACTERISTICS

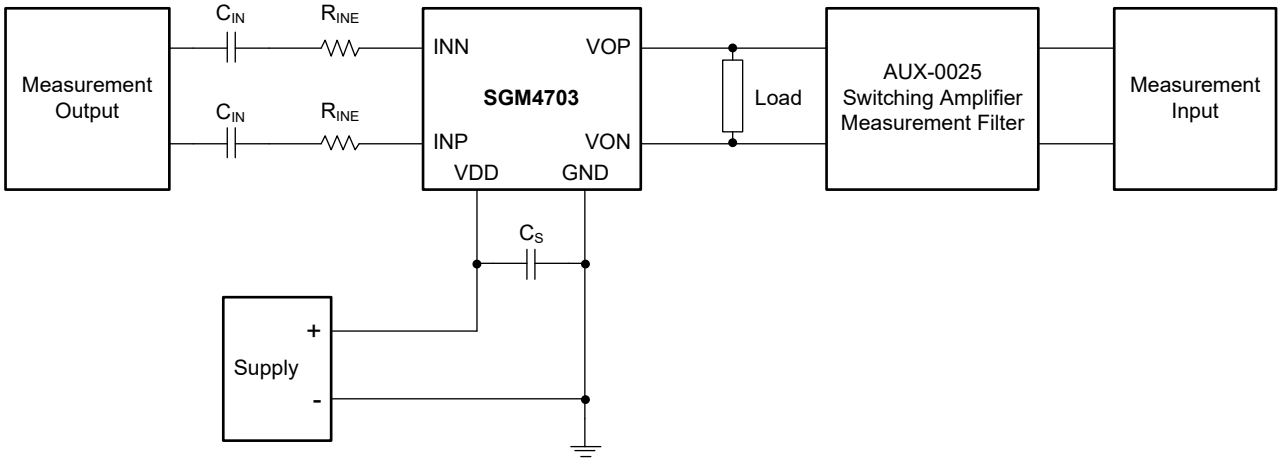


Figure 2. Test Setup Diagram

All parameters specified in Electrical and Typical Performance Characteristics sections are measured according to the conditions:

1. The two differential inputs are shorted for common-mode input voltage measurement. All other parameters are taken with input resistors R_{INE} = 0kΩ and input capacitors C_{IN} = 1μF, unless otherwise specified.

2. The supply decoupling capacitors C_S = 2 × (10nF + 1μF + 220μF) are placed close to the device.

3. A 33μH inductor was placed in series with the load resistor to emulate a speaker load for all AC and dynamic parameters.

ELECTRICAL CHARACTERISTICS

(Minimum and Maximum values are at T_A = -40℃ to +85℃, V_{DD} = 12V, f = 1kHz, Load = 4Ω + 33μH, C_{IN} = 4 × 1μF, R_{INE} = 4 × 0Ω, GAIN = NC (A_V = 26dB), FREQ = NC (f_{PWM} = 360kHz), MODS = NC (SSM), ALC shorted to GND (ALC-1), V_{PLIMIT} = V_{GVDD}, C_{PVDD} = 2 × (10nF + 1μF + 220μF), C_{AVDD} = 1μF, C_{GVDD} = 1μF, C_B = 4 × 0.1μF, both channels driven, typical values are measured at T_A = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	PVDD, AVDD		5		26	V
Supply Quiescent Current	I_{VDD}	V_{PVDD} = 12V, Inputs AC-grounded, No Load			15		mA
		V_{PVDD} = 26V, Inputs AC-grounded, No Load			22	37	
Mute Current	I_{MUTE}	PLIMIT = GND, No Load			8	12	mA
Shutdown Current	I_{SD}	V_{PVDD} = 26V, V_{EN} = 0V	SSM, MODS = NC		55	100	μA
			DSM, MODS = GND		70	120	
Supply Voltage UVLO Detection	V_{UVLOUP}	V_{DD} Rising			4.60	4.85	V
Supply Voltage UVLO Release	V_{UVLODN}	V_{DD} Falling		4.00	4.30		V
Supply Voltage OVP Detection	V_{OVPUP}	V_{DD} Rising			28.0	30.5	V
Supply Voltage OVP Release	V_{OVPDN}	V_{DD} Falling		25.0	26.5		V
Voltage Regulator Output	V_{GVDD}	No Load			5.6		V
Input Common-Mode Bias	V_{COMM}	INPL/R, INNL/R			2.8		V
Digital Low Input Voltage	V_{IL}	EN, MODS				0.8	V
Digital High Input Voltage	V_{IH}	EN		2		V_{AVDD}	V
		MODS		2		V_{GVDD}	
Digital Low Output Voltage	V_{OL}	FAULTB, R_{PULLUP} = 100kΩ, V_{DD} = 18V				0.25	V
Pull-Down Resistor to Ground	R_{DOWN}	EN, MODS, ALC, GAIN, FREQ			250		kΩ
Pull-Up Resistor to GVDD	R_{UP}	MODS			250		kΩ
Output Resistance in Shutdown	R_{OUT-SD}	At VOPL/R, VONL/R, EN = Low			5		kΩ
Voltage Level at GAIN, FREQ, ALC Pins	V_{GAIN}, V_{FREQ}, V_{ALC}	Open			2.5		V
		Shorted to GND			0		
		68kΩ to GND			0.55		
		300kΩ to GND			1.4		
Internal Input Resistance at INPL/R, INNL/R Pins	R_{INI}	Open			30		kΩ
		R_{GAIN} = 0kΩ			20		
		R_{GAIN} = 68kΩ			12		
		R_{GAIN} = 300kΩ			60		
Voltage Gain	A_V	Open			26		dB
		R_{GAIN} = 0kΩ			30		
		R_{GAIN} = 68kΩ			34		
		R_{GAIN} = 300kΩ			20		
PWM Frequency	f_{SW}	Open or R_{FREQ} = 0kΩ			360		kHz
		R_{FREQ} = 68kΩ or R_{FREQ} = 300kΩ			500		
Over-Current Limit	I_{LIMIT}	Dual BTL Configuration			8.8		A/CH
		PBTL Configuration			13		A
Over-Temperature Threshold	T_{OTSD}				160		℃
Over-Temperature Hysteresis	T_{HYS}				20		℃

ELECTRICAL CHARACTERISTICS (continued)

(Minimum and Maximum values are at T_A = -40℃ to +85℃, V_{DD} = 12V, f = 1kHz, Load = 4Ω + 33μH, C_{IN} = 4 × 1μF, R_{INE} = 4 × 0Ω, GAIN = NC (A_V = 26dB), FREQ = NC (f_{PWM} = 360kHz), MODS = NC (SSM), ALC shorted to GND (ALC-1), V_{PLIMIT} = V_{GVDD}, C_{PVDD} = 2 × (10nF + 1μF + 220μF), C_{AVDD} = 1μF, C_{GVDD} = 1μF, C_B = 4 × 0.1μF, both channels driven, typical values are measured at T_A = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Class-D Amplifier (V_{DD} = 12V, R_L = 4Ω + 33μH, Both Channels Driven)							
Maximum Output Power	$P_{O,MAX}$	THD+N = 1%			15		W/CH
ALC Output Power	$P_{O,ALC}$	V_{IN} = 0.50V_{RMS}			13		W/CH
Total Harmonic Distortion + Noise	THD+N	P_O = 1W/CH, Non-ALC Mode	SSM		0.04		%
			DSM		0.02		
		P_O = 10W/CH, Non-ALC Mode	SSM		0.02		
			DSM		0.02		
		V_{IN} = 0.50V_{RMS}, ALC Mode	SSM		0.3		
			DSM		0.3		
Power Efficiency	η	P_O = 10W/CH, Non-ALC Mode			86		%
		V_{IN} = 0.50V_{RMS}, ALC Mode			87		
Output Offset Voltage	V_{OS}	No Load			±20		mV
Idle-Channel Noise	V_N	Inputs AC-Grounded, A-weighted			145		μV_{RMS}
Signal-to-Noise Ratio	SNR	Maximum Output (7V_{RMS}), A-weighted			94		dB
Power Supply Rejection Ratio	PSRR	SSM	f = 1kHz		80		dB
		DSM	f = 1kHz		60		
Common Mode Rejection Ratio	CMRR	f = 1kHz, V_{IN} = 0.2V_{RMS}			60		dB
Channel Separation	Crosstalk	P_O = 10W, f = 1kHz			85		dB
Maximum ALC Attenuation	A_{MAX}	V_{DD} = 12V			12		dB
		V_{DD} = 15V			10		
		V_{DD} = 18V			8.5		
Startup Time	$t_{STARTUP}$	Including Fade-In Time			45		ms
Shutdown Settling Time	t_{SD}	Including Fade-Out Time, T_A = +25℃		10			ms
DC Current Protection (DCP)							
DC-Detect Threshold	V_{DCP}	V_{DD} = 12V, Load = 4Ω + 33μH			2.4		V
		V_{DD} = 15V, Load = 4Ω + 33μH			3.0		
		V_{DD} = 18V, Load = 4Ω + 33μH			3.6		
Fade-In and Fade-Out							
Fade-In Time	t_{FADEIN}				8		ms
Fade-Out Time	$t_{FADEOUT}$				5		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 15V, f = 1kHz, Load = 4Ω + 33μH, SSM, both channels driven, T_A = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Output Power (1)	$P_{O,PEAK}$	THD+N = 10%, Non-ALC Mode		27		W/CH
		THD+N = 1%, Non-ALC Mode		23		
ALC Output Power	$P_{O,ALC}$	V_{DD} = 15V, V_{IN} = 0.60V_{RMS}		21		W/CH
Total Harmonic Distortion + Noise	THD+N	P_O = 15W/CH, Non-ALC Mode		0.02		%
		V_{IN} = 0.60V_{RMS}, ALC Mode		0.3		
Power Efficiency (2)	η	P_O = 15W/CH, Non-ALC Mode		85		%
		V_{IN} = 0.60V_{RMS}, ALC Mode		86		
Signal-to-Noise Ratio	SNR	P_O = 20W/CH, A-weighted		95		dB

(V_{DD} = 18V, f = 1kHz, Load = 8Ω + 33μH, SSM, both channels driven, T_A = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Output Power (1)	$P_{O,PEAK}$	THD+N = 10%, Non-ALC Mode		22		W/CH
		THD+N = 1%, Non-ALC Mode		18		
ALC Output Power	$P_{O,ALC}$	V_{IN} = 0.70V_{RMS}		16		W/CH
Total Harmonic Distortion + Noise	THD+N	P_O = 10W/CH, Non-ALC Mode		0.02		%
		V_{IN} = 0.70V_{RMS}, ALC Mode		0.3		
Power Efficiency (2)	η	P_O = 10W/CH, Non-ALC Mode		90		%
		V_{IN} = 0.70V_{RMS}, ALC Mode		91		
Signal-to-Noise Ratio	SNR	P_O = 15W/CH, A-weighted		97		dB

(V_{DD} = 24V, f = 1kHz, Load = 8Ω + 33μH, SSM, both channels driven, T_A = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Output Power (1)	$P_{O,PEAK}$	THD+N = 10%, Non-ALC Mode		40		W/CH
		THD+N = 1%, Non-ALC Mode		32		
ALC Output Power	$P_{O,ALC}$	V_{IN} = 1.0V_{RMS}		30		W/CH
Total Harmonic Distortion + Noise	THD+N	P_O = 20W/CH, Non-ALC Mode		0.02		%
		V_{IN} = 1.0V_{RMS}, ALC Mode		0.3		
Power Efficiency (2)	η	P_O = 20W/CH, Non-ALC Mode		90		%
		V_{IN} =1.0V_{RMS}, ALC Mode		91		
Signal-to-Noise Ratio	SNR	P_O = 25W/CH, A-weighted		98		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 24V, f = 1kHz, Load = 4Ω + 33μH, SSM, PBTL configuration, T_A = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Output Power (1)	$P_{O,PEAK}$	THD+N = 10%, Non-ALC Mode		80		W
		THD+N = 1%, Non-ALC Mode		64		
ALC Output Power	$P_{O,ALC}$	V_{IN} = 1.0V_{RMS}		60		W
Total Harmonic Distortion + Noise	THD+N	P_O = 40W, Non-ALC Mode		0.1		%
		V_{IN} = 1.0V_{RMS}, ALC Mode		0.3		
Power Efficiency (2)	η	P_O = 40W, Non-ALC Mode		90		%
		V_{IN} = 1.0V_{RMS}, ALC Mode		91		
Signal-to-Noise Ratio	SNR	P_O = 50W, A-weighted		98		dB

(V_{DD} = 15V, f = 1kHz, Load = 3Ω + 15μH, SSM, PBTL configuration, T_A = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Output Power (1)	$P_{O,PEAK}$	THD+N = 10%, Non-ALC Mode		40		W
		THD+N = 1%, Non-ALC Mode		33		
ALC Output Power	$P_{O,ALC}$	V_{IN} = 0.60V_{RMS}		30		W
Total Harmonic Distortion + Noise	THD+N	P_O = 20W, Non-ALC Mode		0.1		%
		V_{IN} = 0.60V_{RMS}, ALC Mode		0.3		
Power Efficiency (2)	η	P_O = 20W, Non-ALC Mode		89		%
		V_{IN} = 0.60V_{RMS}, ALC Mode		90		
Signal-to-Noise Ratio	SNR	P_O = 30W, A-weighted		96		dB

(V_{DD} = 12V, f = 1kHz, Load = 2Ω + 15μH, SSM, PBTL configuration, T_A = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Output Power (1)	$P_{O,PEAK}$	THD+N = 10%, Non-ALC Mode		37		W
		THD+N = 1%, Non-ALC Mode		30		
ALC Output Power	$P_{O,ALC}$	V_{IN} = 0.50V_{RMS}		27		W
Total Harmonic Distortion + Noise	THD+N	P_O = 20W, Non-ALC Mode		0.1		%
		V_{IN} = 0.50V_{RMS}, ALC Mode		0.3		
Power Efficiency (2)	η	P_O = 20W, Non-ALC Mode		87		%
		V_{IN} = 0.50V_{RMS}, ALC Mode		88		
Signal-to-Noise Ratio	SNR	P_O = 25W, A-weighted		94		dB

NOTES:

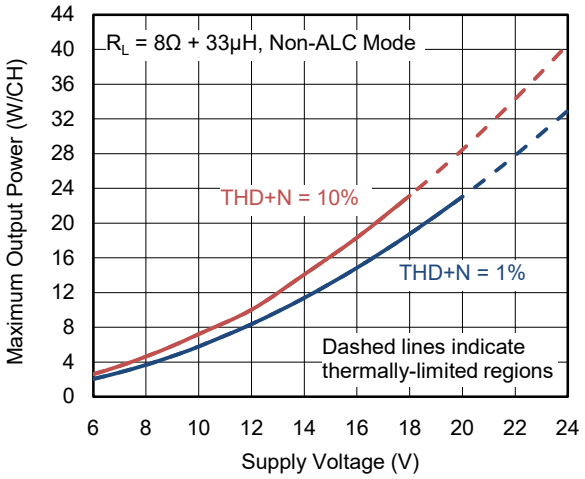
1. The peak output power is defined as an instantaneous maximum output power with no consideration of the thermal dissipation capability of the system board. The maximum continuous output power will be less than the peak output power and largely depend upon the thermal dissipation capability of the system board.

2. All the power efficiency data are given for a two-side, two-layer printed circuit board and shall be used for reference only. The power efficiency will be strongly affected by the thermal dissipation capability of the system board, such as the number of layers and the application of a heat sink.

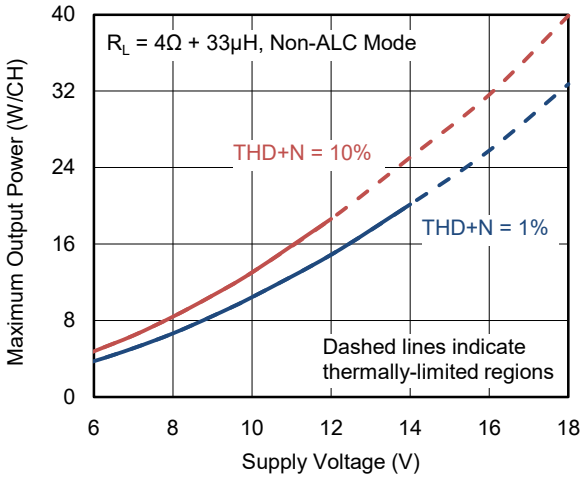
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, f = 1kHz, C_{IN} = 4 × 1μF, A_V = 26dB, f_{PWM} = 360kHz, SSM Mode, V_{PLIMIT} = V_{GVDD}, both channels driven (BTL Mode), unless otherwise specified.

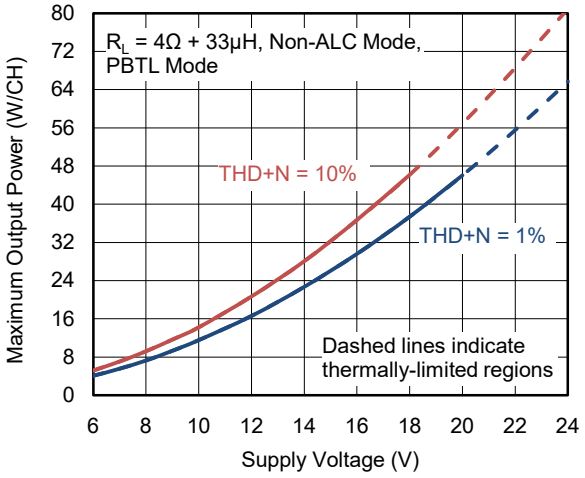
Maximum Output Power vs. Supply Voltage



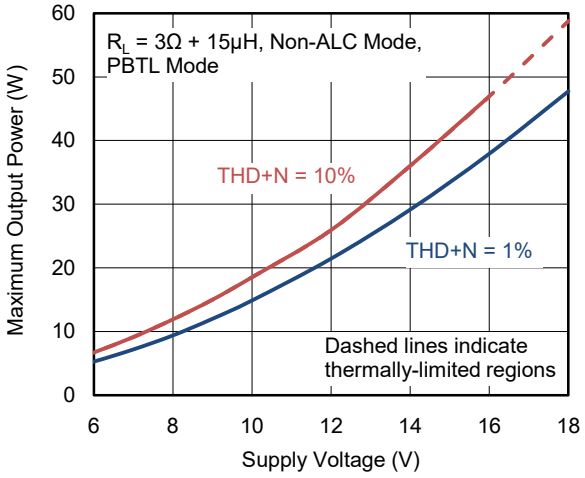
Maximum Output Power vs. Supply Voltage



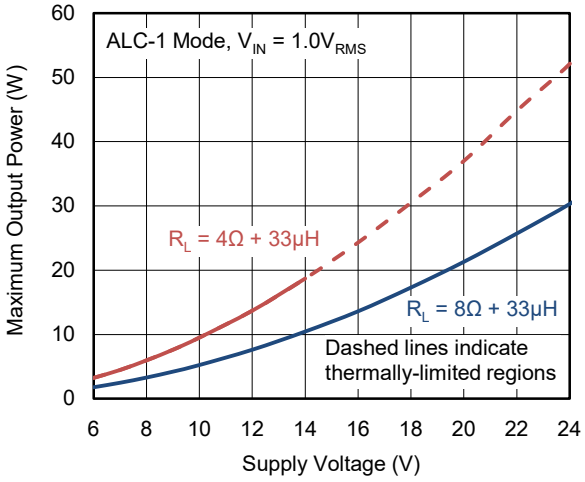
Maximum Output Power vs. Supply Voltage



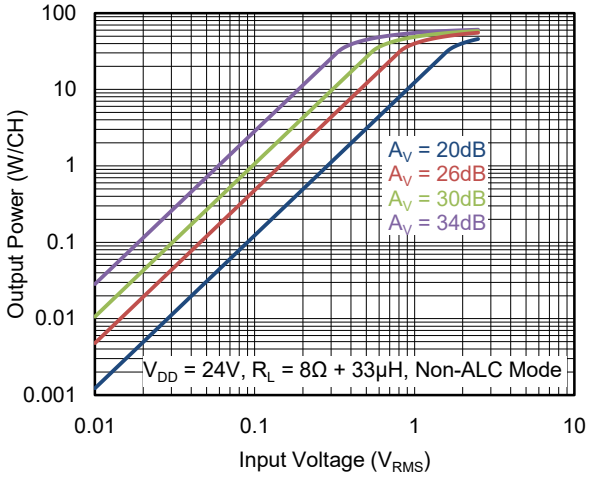
ALC Output Power vs. Supply Voltage



ALC Output Power vs. Supply Voltage



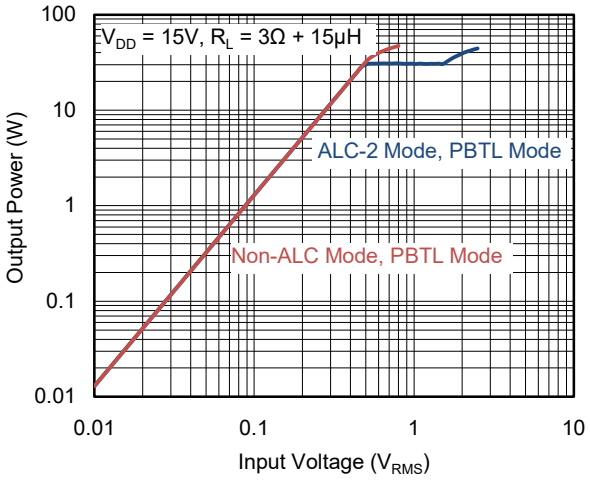
Output Power vs. Input Voltage



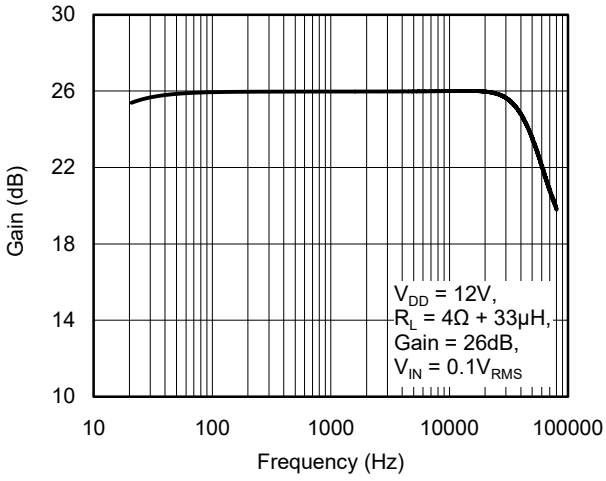
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, f = 1kHz, C_{IN} = 4 × 1μF, A_V = 26dB, f_{PWM} = 360kHz, SSM Mode, V_{PLIMIT} = V_{GVDD}, both channels driven (BTL Mode), unless otherwise specified.

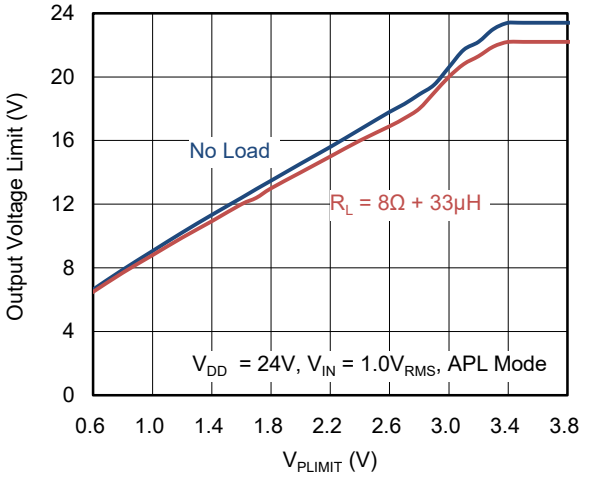
Output Power vs. Input Voltage



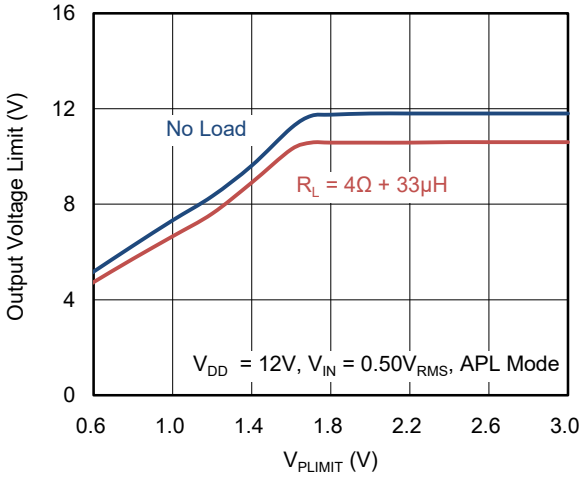
Gain vs. Frequency



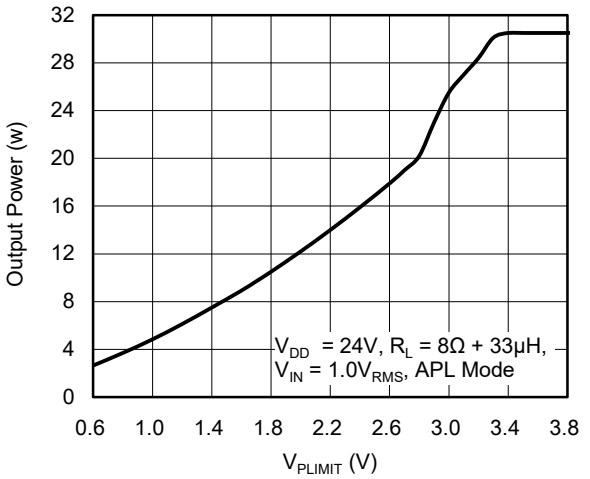
Output Voltage Limit vs. V_{PLIMIT}



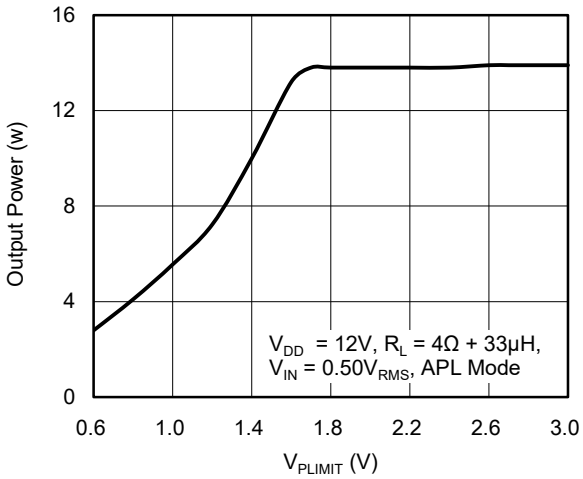
Output Voltage Limit vs. V_{PLIMIT}



Output Power vs. V_{PLIMIT}



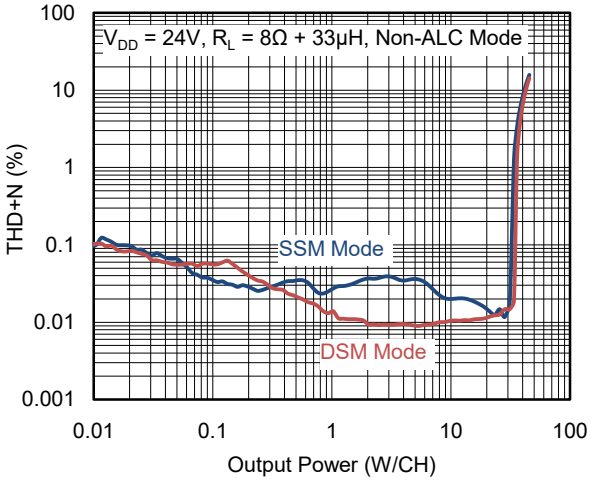
Output Power vs. V_{PLIMIT}



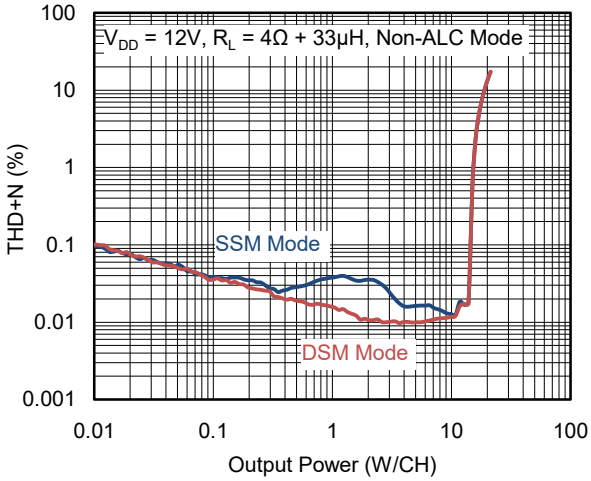
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, f = 1kHz, C_{IN} = 4 × 1μF, A_V = 26dB, f_{PWM} = 360kHz, SSM Mode, V_{PLIMIT} = V_{GVDD}, both channels driven (BTL Mode), unless otherwise specified.

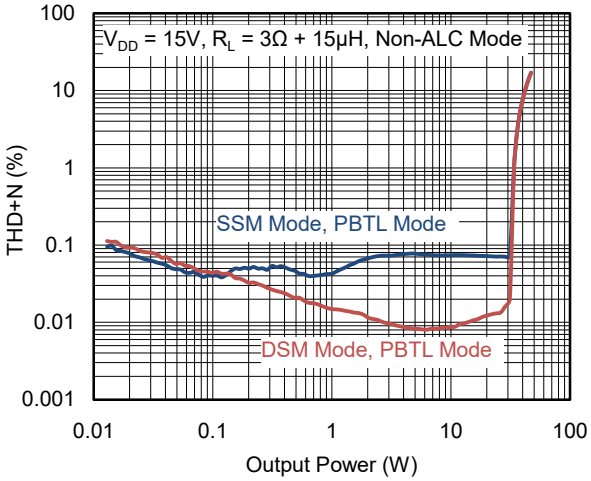
THD+N vs. Output Power



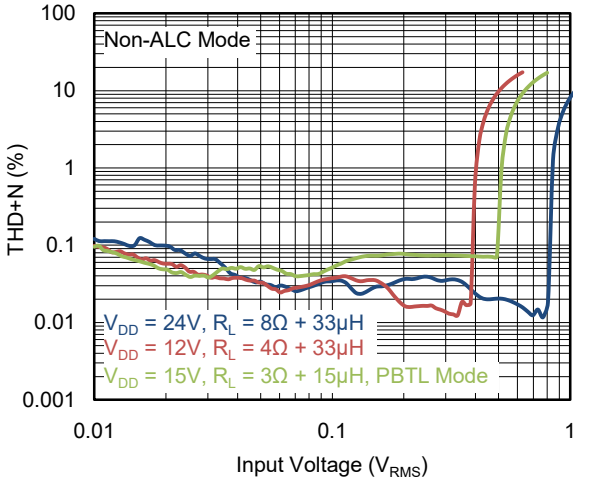
THD+N vs. Output Power



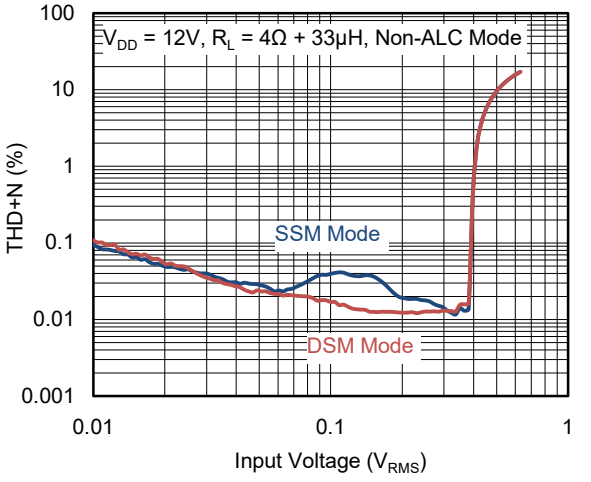
THD+N vs. Output Power



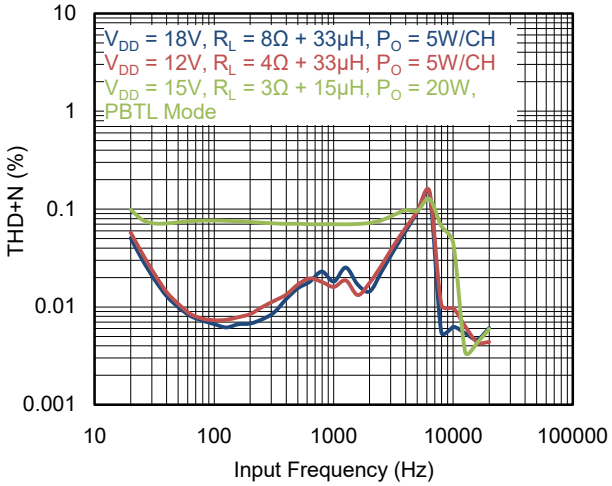
THD+N vs. Input Voltage



THD+N vs. Input Voltage



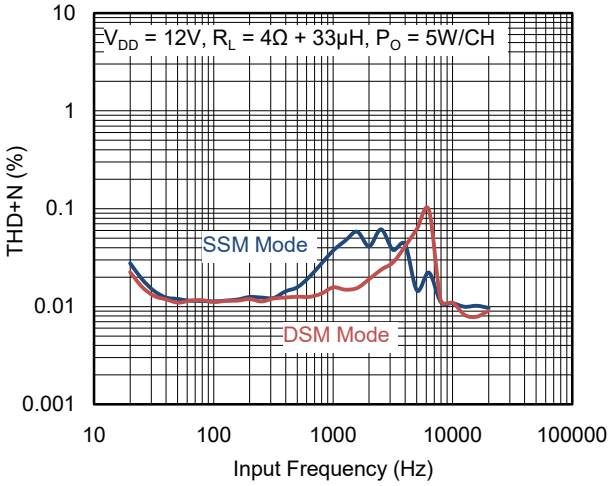
THD+N vs. Input Frequency



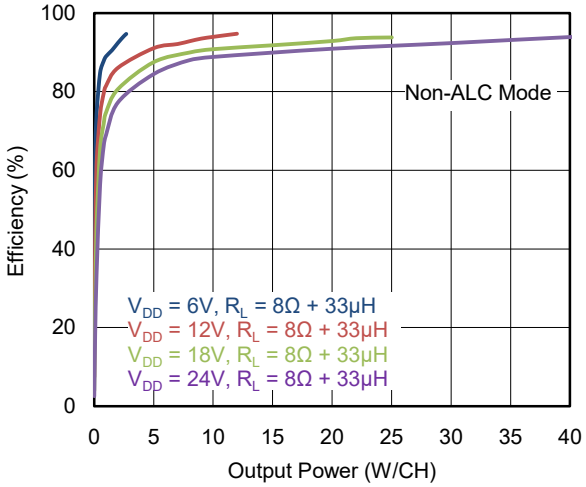
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, f = 1kHz, C_{IN} = 4 × 1μF, A_V = 26dB, f_{PWM} = 360kHz, SSM Mode, V_{PLIMIT} = V_{GVDD}, both channels driven (BTL Mode), unless otherwise specified.

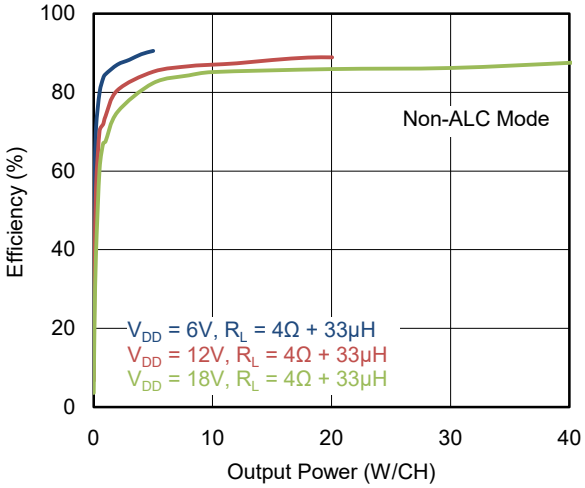
THD+N vs. Input Frequency



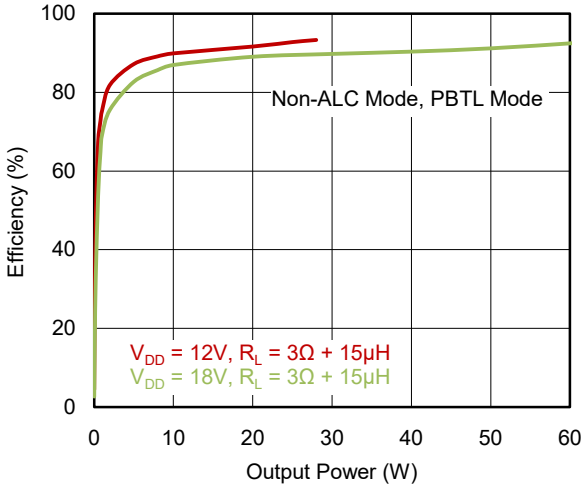
Efficiency vs. Output Power



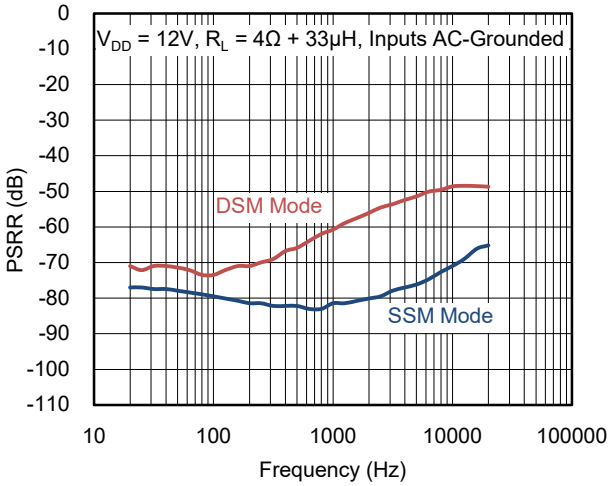
Efficiency vs. Output Power



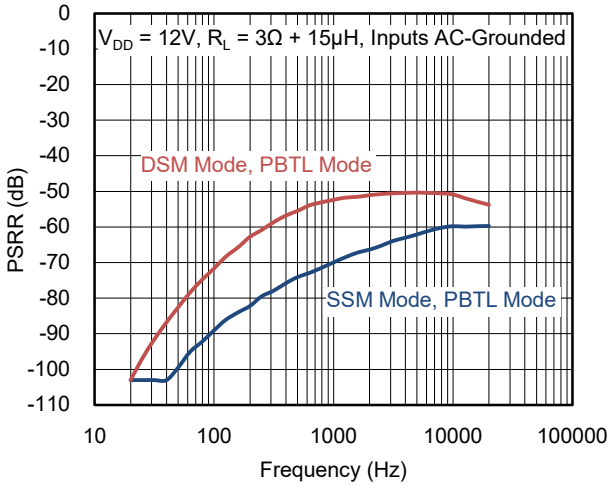
Efficiency vs. Output Power



PSRR vs. Input Frequency



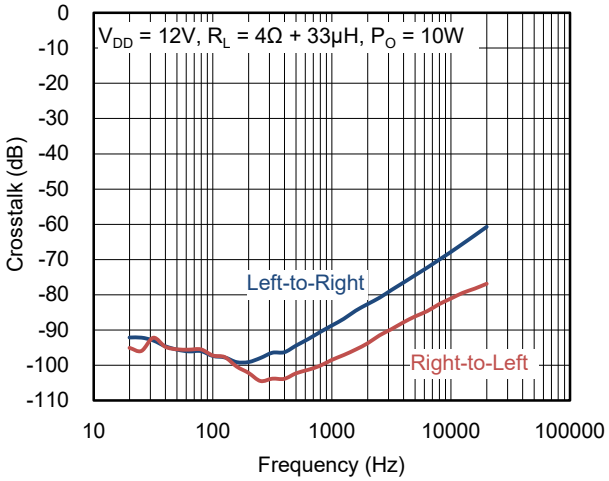
PSRR vs. Input Frequency



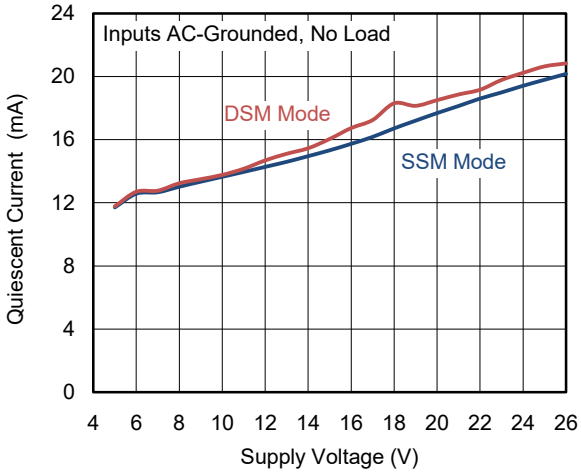
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, f = 1kHz, C_{IN} = 4 × 1μF, A_V = 26dB, f_{PWM} = 360kHz, SSM Mode, V_{PLIMIT} = V_{GVDD}, both channels driven (BTL Mode), unless otherwise specified.

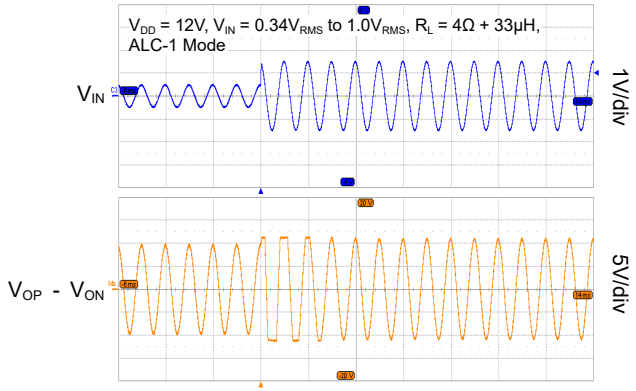
Crosstalk vs. Input Frequency



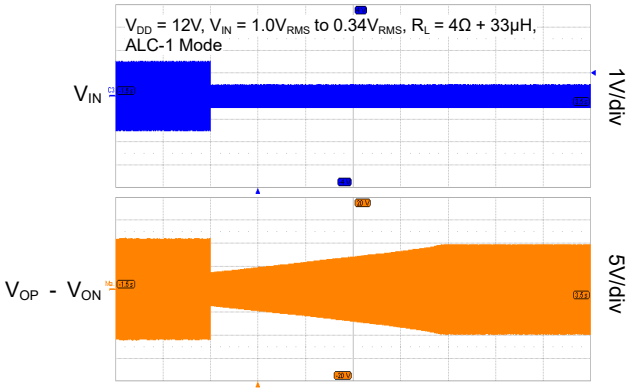
Quiescent Current vs. Supply Voltage



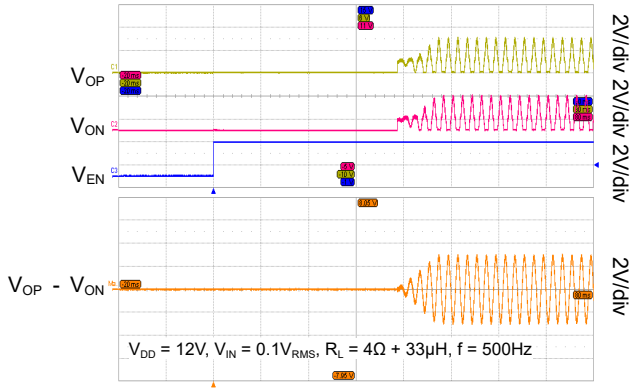
Audio Outputs during ALC Attack



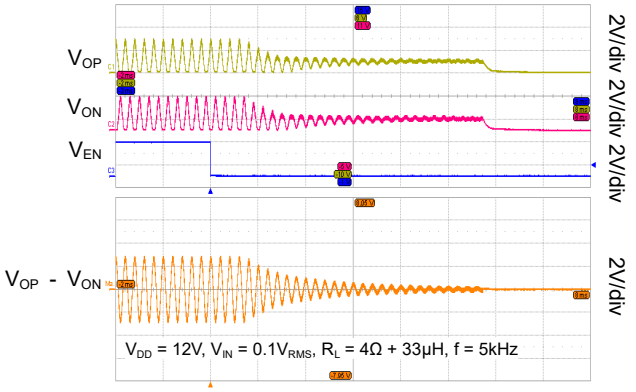
Audio Outputs during ALC Release



Audio Outputs during Startup



Audio Outputs during Shutdown



FUNCTIONAL BLOCK DIAGRAM

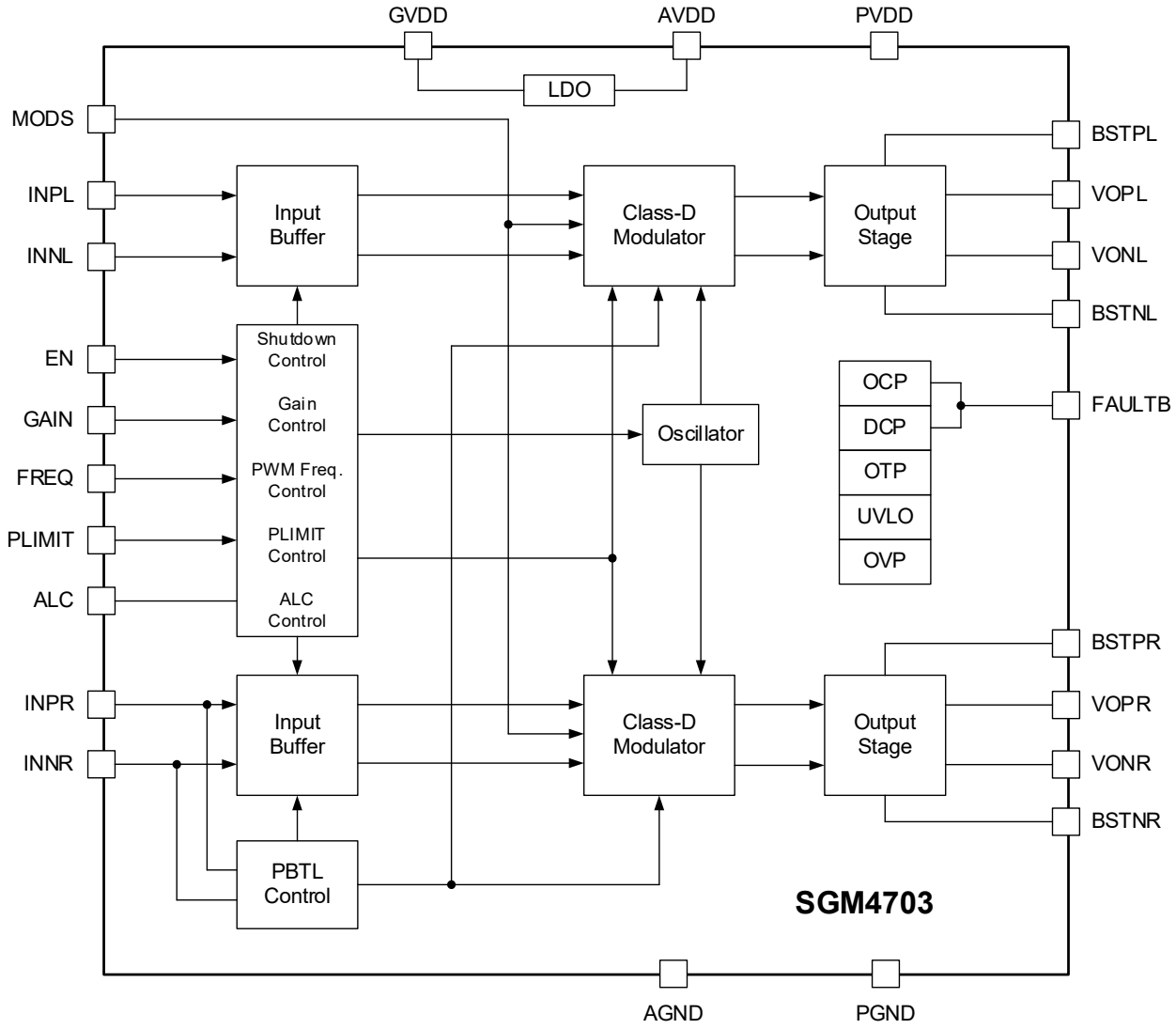


Figure 3. Block Diagram

APPLICATION INFORMATION

The SGM4703 is a high-power, high efficiency, stereo Class-D audio power amplifier with adjustable power limit (APL) and automatic level control (ALC). It operates with a wide range of supply voltages from 5V to 26V. With 24V supply voltage, it can deliver 2 × 40W peak output power for a pair of 8Ω speakers with 10% THD+N.

The high efficiency of SGM4703 extends battery life in playing music and allows it to deliver an output power of 2 × 20W without the need for a bulky heat sink on a two-layer system board. Its high PSRR and low EMI emission reduce system design and manufacturing complexities, as well as thus lower system cost.

The SGM4703 features APL and ALC. The APL limits peak audio outputs to a user-defined value to protect audio speakers from excessive power dissipation and over-load. The APL and ALC adjust the voltage gain of the audio amplifiers in response to over-limit audio inputs, eliminating output clipping distortion while maintaining a maximally allowed dynamic range of audio outputs. The limiting voltage of APL and ALC can be either the supply voltage or a user-defined value.

The SGM4703 can be configured into driving either a pair of speakers in Bridge-Tied-Load (BTL) configuration for stereo applications or a single speaker in Parallel BTL (PBTL) configuration for mono applications. In PBTL configuration, with 15V supply voltage, it can deliver into a 3Ω speaker an output power of 33W with 1% THD+N, or an ALC output power of 30W with THD+N less than 0.5%.

The SGM4703 features two PWM modulation schemes for use in Class-D audio amplifiers: Dual-Side-Modulation (DSM) and Single-Side-Modulation (SSM), allowing for system optimization for higher efficiency or lower THD.

The SGM4703 includes comprehensive protection modes against various operating faults including under-voltage, over-voltage, over-current, over-temperature, and DC-detect for safe and reliable operation.

Operating Mode Control

The SGM4703 features APL and ALC modes of operation. In APL mode, peak audio outputs are clamped (hard-limited) to a voltage level defined by the PLIMIT pin, protecting audio speakers from excessive power dissipation and over-load.

As described in Table 1, depending upon the pin voltage at PLIMIT and the pin configuration at ALC, the SGM4703 can be configured into one of four operating modes: Mute, APL, ALC, and Traditional. In SGM4703, the pin voltage at PLIMIT, V_{PLIMIT}, defines the limiting voltage of audio outputs for both APL and ALC modes.

If V_{PLIMIT} is set less than 0.3V, the device operates in mute mode regardless of the pin configuration at ALC.

If V_{PLIMIT} is set higher than 4.5V with the ALC pin unconnected, the device operates in a traditional Class-D mode without APL or ALC. In this mode, the output clipping distortion will occur as peak output voltages reach to the supply voltage PVDD.

If V_{PLIMIT} is set in the range from 0.7V to 3.5V with the ALC pin connected to ground through an external resistor of 0kΩ, 68kΩ or 300kΩ, the device operates in APL mode. The audio outputs in APL mode are limited to a value approximately equal to ($6 \times V_{PLIMIT}$).

If V_{PLIMIT} is set higher than 4.5V with the ALC pin connected to ground through an external resistor of 0kΩ, 68kΩ, or 300kΩ, the device operates in ALC mode and the limiting voltage of audio outputs is internally set at the supply voltage. Thus, the peak voltage of audio outputs is limited to a value that is substantially close to PVDD.

Table 1. Operating Mode Control

V_{PLIMIT}	R_{ALC}	Mode	Description
V_{PLIMIT} < 0.3V	X	Mute	Audio outputs shorted to PGND.
V_{PLIMIT} < 4.5V	Open	X	Not applicable.
V_{PLIMIT} > 4.5V		Traditional	No APL and No ALC.
0.7V < V_{PLIMIT} < 3.5V	0kΩ, 68kΩ or 300kΩ to GND	APL	Audio outputs limited to a value defined by V_{PLIMIT}.
V_{PLIMIT} > 4.5V		ALC	Audio outputs limited to the supply voltage PVDD.

APPLICATION INFORMATION (continued)

Figure 4 depicts large audio outputs in different operating modes when excessive inputs are applied to cause peak outputs higher than either the supply voltage or a user-defined voltage limit lower than the supply voltage.

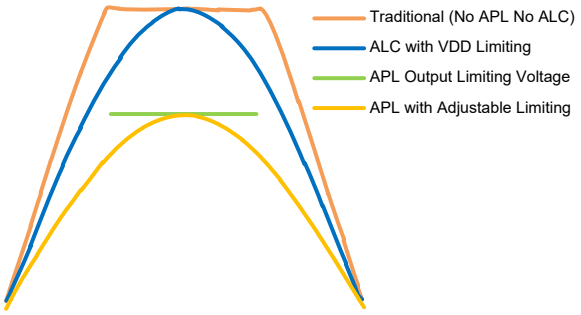


Figure 4. Large Audio Outputs in Different Operating Modes

GVDD Supply

The GVDD is an internally generated supply voltage for internal circuitry. It is also used as the supply voltage for the resistor divider to set the voltage at the PLIMIT pin. It is highly suggested to decouple the GVDD pin with a 1μF ceramic capacitor to ground for stable operation. Note that the current drawn from the GVDD pin by external circuitry, including all the resistor dividers at ALC, GAIN, FREQ, and PLIMIT pins, must be kept less than 5mA.

MUTE Control

The SGM4703 can be configured into mute mode when the PLIMIT pin is pulled low by an inverting transistor, as shown in Figure 5. In mute mode, the output stages of both audio amplifiers are in Hi-Z and the differential audio outputs (VOPL/R and VONL/R) are pulled to ground through on-chip resistors respectively. To restore to its normal operation, the output of the inverting transistor is reverted to Hi-Z state, allowing the resistor divider (from GVDD to ground) tapped at the PLIMIT pin to set the voltage limit for APL.

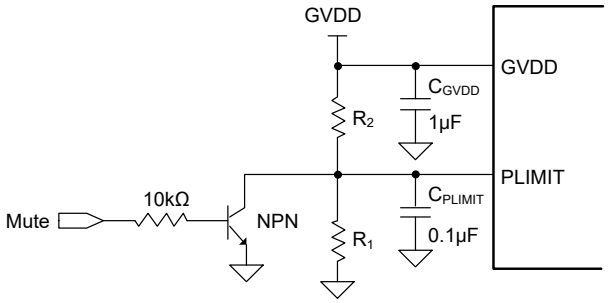


Figure 5. Example Circuit Diagram of Mute Control

Automatic Level Control (ALC)

The automatic level control is to maintain the audio outputs for a maximum voltage swing without clip distortion when excessive inputs that may cause output clipping are applied. With ALC, the SGM4703 lowers the voltage gain of both audio amplifiers to an appropriate value such that output clipping is substantially eliminated.

In Figure 6, “Attack” is the duration where the voltage gain of the audio amplifiers decreases until output clipping is substantially eliminated. “Release” is the duration where the voltage gain of the audio amplifiers recovers (increases) until it reaches to a value that is maximally allowed without output clipping.

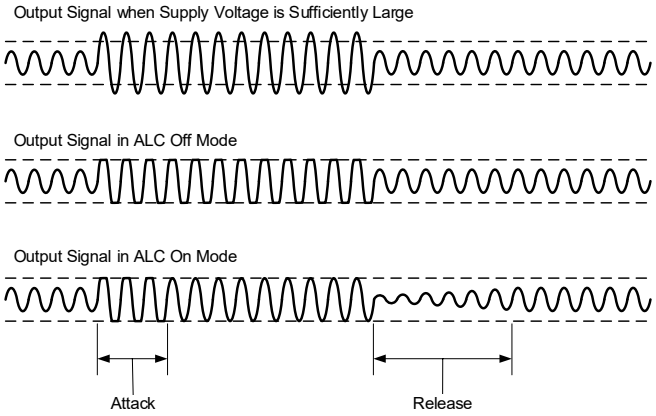


Figure 6. Automatic Level Control Diagram

ALC Mode Select

The SGM4703 can be configured into ALC or Non-ALC mode via the ALC pin, as described in Table 2. When the ALC pin is left unconnected, the SGM4703 operates in Non-ALC mode. The Non-ALC mode is typically chosen for applications where maximum audio loudness is desired and the amount of output clipping distortions can be measurably controlled at the audio source. In other pin configurations, the SGM4703 operates in ALC mode with three specific audio dynamic characteristics. For most applications, the ALC mode is preferred for its capability to substantially eliminate output clipping distortion, excessive power dissipation and speaker over-load.

APPLICATION INFORMATION (continued)

Three sets of ALC dynamic characteristics can be selected for specific sound effects, as described in Table 2. The ALC-1 mode (the ALC pin shorted to GND) plays music in a most mellow manner with negligible amount of clipping distortion and lower average output power. On the other hand, the ALC-3 mode (the ALC pin shorted to GND via a 300kΩ resistor) plays music in a most dynamic manner with some extent of clipping distortion and higher average output power (loudness).

Table 2. ALC Mode Select

ALC Pin Configuration	ALC Mode	Sound Effects	
		Loudness	Output Clipping Distortion
Open	Non-ALC	Potentially highest loudness	No control on output clipping
Shorted to GND	ALC-1	Most mellow sound (Lowest loudness under ALC)	Negligible output clipping
68kΩ to GND	ALC-2	Medium loudness	Slight output clipping
300kΩ to GND	ALC-3	Most dynamic sound (Highest loudness under ALC)	Acceptable output clipping
Note: The resistor tolerance of R_{ALC} should be 5% or better.			

Voltage Gain Setting

To accommodate various application requirements, the SGM4703 features 4 selectable voltage gains for audio amplifiers. An external resistor R_{GAIN} from the GAIN pin to ground sets the voltage gain, as shown in Table 3.

Although the voltage gains as described in Table 3 vary a little (less than 2%) from parts to parts, the input impedances at the same voltage gain may vary by ±20% over parts, due to process variations in the actual resistance of the input resistors. For design purposes, the input impedance should be assumed to be 10kΩ, which is the absolute minimum input impedance of the audio amplifiers in SGM4703. At lower gain settings, the input impedance could be as high as 60kΩ.

Table 3. Voltage Gain Select

GAIN Pin Configuration	R_{INI} (kΩ)	A_V (V/V)	A_V (dB)
Open	30	20	26
Shorted to GND	20	30	30
68kΩ to GND	12	50	34
300kΩ to GND	60	10	20
Note: The resistor tolerance of R_{GAIN} should be 5% or better.			

The voltage gain of the audio amplifiers can be slightly adjusted by inserting small external input resistors R_{INE}, in series with the input capacitors C_{IN}, as depicted in Figure 7 and Figure 8 for differential and single-ended inputs respectively. In the figures, it is required that $C_{IN} = C_{INL1/2} = C_{INR1/2}$ and $R_{INE} = R_{INL1/2} = R_{INR1/2}$.

As depicted in Figure 8, the unused inputs of SGM4703 in single-ended inputs applications must be AC-grounded at the audio source. Also, take care to match the impedances of two differential inputs.

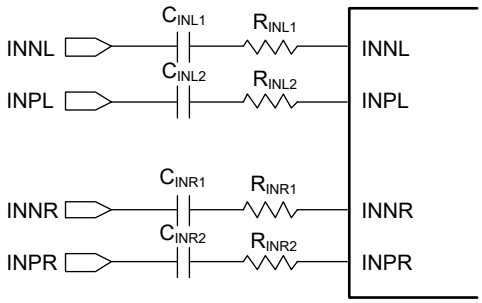


Figure 7. Gain Setting (Differential Inputs)

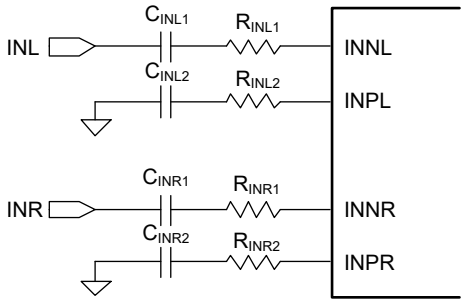


Figure 8. Gain Setting (Single-Ended Inputs)

The value of R_{INE} (in kΩ) for a given voltage gain can be calculated by Equation 1, where A_V is the voltage gain of the audio amplifier.

$$A_V = \frac{600}{R_{INE} + R_{INI}} \quad (1)$$

The choice of the voltage gain will strongly influence the loudness and quality of audio sounds. In general, the higher the voltage gain is, the louder the sound is perceived. However an excessive voltage gain may cause audio outputs to be severely clipped (Non-ALC mode) or compressed (ALC mode) for high-level (loud) audio sounds. On the other hand, an unusually low gain may cause relatively low-level (quite) sounds soft or inaudible. Thus it is crucial to choose a proper voltage gain for well balanced audio quality.

APPLICATION INFORMATION (continued)

The voltage gain is chosen based upon various system-level considerations including the supply voltage, the dynamic range of audio sources and speaker loads, and the desired sound effects. As a general guideline, the voltage gain can be simply expressed in Equation 2. In the equation, $V_{IN,MAX}$ (in V_{RMS}) is the maximum input level from the audio source, PVDD (in volts) is the supply voltage, and α is the design parameter, which ranges from 0.66 to 1.0. The higher α is, the higher the average output power (louder) is, with some degree of compression for high-level audio sounds.

$$A_V = \frac{\alpha \times PVDD}{V_{IN,MAX}} \quad (2)$$

As an example, Table 4 shows the voltage gain for various input levels with PVDD at 12V, 18V and 24V and α at about 0.80. In this table, R_{INE} is the external input resistor in series with the input capacitor and R_{INI} is the internal input resistor.

Table 4. Typical Voltage Gain Settings for Various V_{DD} & Audio Input Levels

$V_{IN, MAX}$ (V_{RMS})	A_V (V/V)	A_V (dB)	R_{GAIN} to GND (kΩ)	R_{INI} (kΩ)	R_{INE} (kΩ)
V_{DD} = 12V					
0.5	20	26	Open	30	0
0.7	13.3	22.5	Open	30	15
1.0	10	20	300	60	0
V_{DD} = 18V					
0.5	30	29.5	0	20	0
0.7	20	26	Open	30	0
1.0	15	23.5	Open	30	10
V_{DD} = 24V					
0.5	40	32	68	12	3.0
0.7	28.5	29	0	20	1.0
1.0	20	26	Open	30	0

PWM Frequency Setting

To accommodate various application requirements, the SGM4703 features two selectable PWM frequencies with optional spread-spectrum for the Class-D audio amplifiers. An external resistor R_{FREQ} from the FREQ pin to ground sets the PWM frequency and optional spread-spectrum, as shown in Table 5.

Table 5. PWM Frequency Select with Optional Spread-Spectrum

FREQ Pin Configuration	PWM Frequency (kHz)	Spread-Spectrum
Open	360	No
Shorted to GND	360	Yes
68kΩ to GND	500	No
300kΩ to GND	500	Yes
Note: The resistor tolerance of R_{FREQ} should be 5% or better.		

PWM Modulation Schemes

To accommodate various application requirements, the SGM4703 features two PWM modulation schemes, i.e., Single-Side-Modulation (SSM) and Double-Side-Modulation (DSM). In typical applications, the SSM scheme is preferred for its lower EMI and higher PSRR and efficiency. The modulation scheme is selected via the MODS pin, as described in Table 6. The PWM modulation scheme is latched during power-up and cannot be changed while the device is in operation.

Table 6. Modulation Scheme Select

MODS	Modulation Schemes
High or Open	Single-Side-Modulation (SSM)
Low	Double-Side- Modulation (DSM)

Double-Side-Modulation (DSM)

With DSM scheme, during an idle condition (no audio signal applied), both VOPL/R and VONL/R outputs are at 50% duty cycle and in phase with each other, resulting in little or no current flowing through the speaker. When a positive audio input is applied, the duty cycle of VOPL/R is greater than 50% and VONL/R is less than 50%, resulting in a positive current flowing through the speaker. When a negative audio input is applied, the duty cycle of VOPL/R is less than 50% and VONL/R is greater than 50%, resulting in a negative current flowing through the speaker. Compared with the traditional modulation scheme, the DSM scheme reduces the switching current, which minimizes any I^2R losses in the speaker load and eliminates the need for an LC output filter for most applications.

APPLICATION INFORMATION (continued)

Single-Side-Modulation (SSM)

The SSM scheme alters the DSM scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required for the selection of the output filter. With SSM scheme, the audio outputs operate with less than 10% modulation during an idle condition. When an audio signal is applied, one output will decrease and another one will increase. The decreasing output signal will quickly rail to ground at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved with SSM scheme due to the reduction of switching losses. The THD penalty with SSM scheme is minimized by the on-chip linear feedback loop.

Volume Fade-In and Fade-Out

The SGM4703 features volume fade-in and fade-out to reduce intermittent sound and eliminate uncomfortable hearing experience during the transitions when the device enters or exits the normal operation. Figure 9 and Figure 10 show the audio output waveforms during fade-in and fade-out respectively.

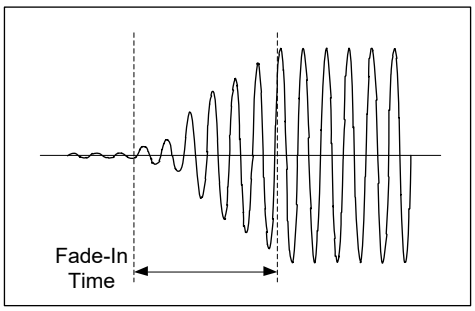


Figure 9. Fade-In Waveform

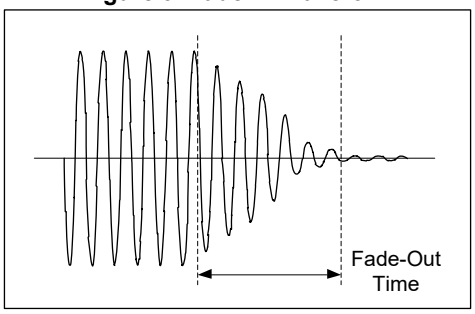


Figure 10. Fade-Out Waveform

PBTL Configuration (Mono Mode)

The SGM4703 features an optional mono mode that allows the left and right channels to operate in parallel BTL configuration. To operate the SGM4703 in mono mode, connect the INNR and INPR pins (pin 11 and 12) directly to ground (no decoupling capacitors). In mono mode, as shown in Figure 11, an audio input signal applied to the left channel (pin 3 and 4) is routed to the H-bridge of both channels. Note that the mono mode is intended to be configured strictly by the hardware connection. Leaving either INNR or INPR pin unconnected while the audio outputs VOPL/R and VONL/R are wired together in PBTL configuration can trigger an over-current or thermal overload protection or both. The mono mode is configured by the following arrangement:

- Connect INPR and INNR pins directly to ground (no decoupling capacitors).
- Connect VOPL to VONL together as one terminal of the speaker and connect VOPR to VONR together as the other terminal of the speaker. Use heavy PCB traces as close as possible to the device.
- Place the speaker between the left and right-channel outputs.
- Apply an audio signal to the left-channel inputs (INPL and INNL pins).

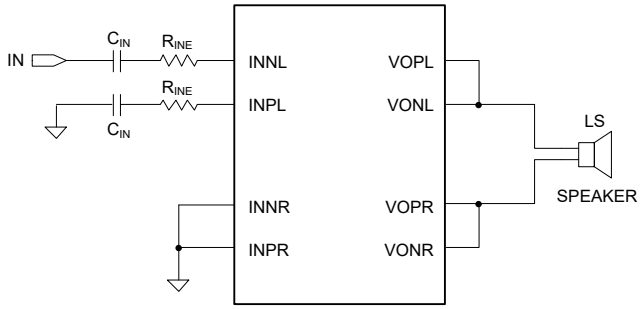


Figure 11. PBTL Configuration for Mono Applications

Click-and-Pop Suppression

The SGM4703 features comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transients internal to the device. When entering into shutdown, the differential audio outputs VOPL/R and VONL/R ramp down to ground simultaneously.

PSRR Enhancement

Without a dedicated pin for the common-mode voltage bias and an external holding capacitor onto the pin, the SGM4703 achieves a PSRR, 80dB at 1kHz with SSM scheme.

APPLICATION INFORMATION (continued)

Startup and Shutdown

The SGM4703 requires a power-up sequence (see Figure 12). Please hold EN low at least 10ms after PVDD and AVDD supply voltages are turned on.

The SGM4703 employs the EN pin to minimize power consumption when not in use. When the EN pin is pulled low, the SGM4703 is forced into shutdown mode. At this time, all the analog circuitry is de-biased and the supply current is reduced to the minimum level, and the differential outputs are shorted to ground through an on-chip resistor (5kΩ) individually. Once in shutdown mode, the EN pin must remain low for at least 10ms (t_{SD}) for the shutdown settling time before it can be pulled high again. When the EN pin is asserted high, the device exits out of shutdown mode and enters into normal operation after the startup time ($t_{STARTUP}$) of 45ms.

An on-chip pull-down resistor of 250kΩ is included onto the EN pin. Thus, shutdown mode is the state when the power supply is first applied to the device. Whenever possible, please hold the EN pin low until the device is properly powered up and the audio signals at the inputs are stable. Also, for best power-off pop performance, place the device in shutdown mode prior to removing the power supply voltage.

Note that the setting at the MODS pin is latched during startup and cannot be changed while the device is in operation. To change the setting of the MODS pin, the device must be first brought into shutdown mode by pulling the EN pin low for at least 10ms before it can be restored to its normal operation.

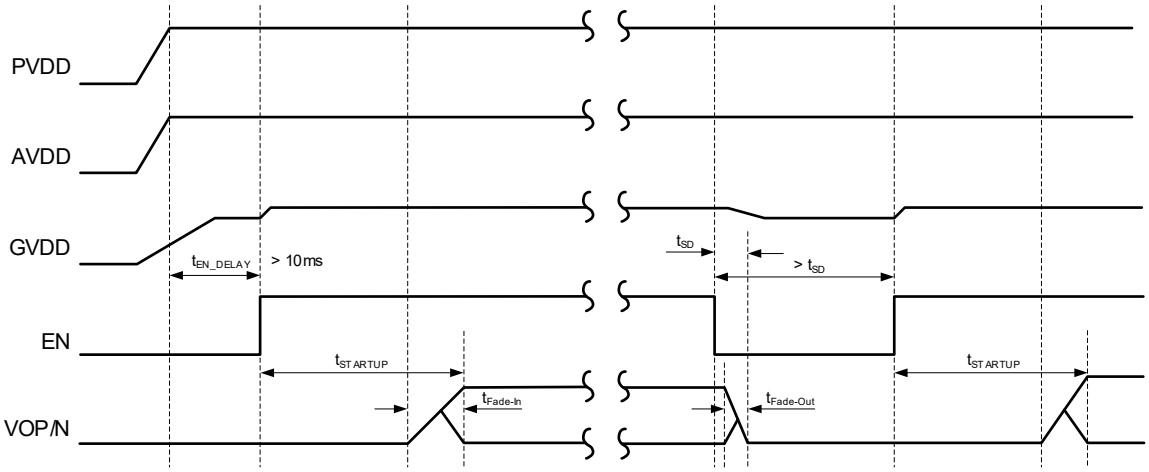


Figure 12. Startup Timming

APPLICATION INFORMATION (continued)

Protection Modes

For safe operation, the SGM4703 incorporates comprehensive protection circuits against various operating faults including Under-Voltage, Over-Voltage, Over-Current, Over-Temperature, and DC-Detect, as described in Table 7. In the shutdown mode, all the analog circuitry is de-biased with differential outputs to be shorted to ground. In the mute mode, all the analog circuitry is enabled with differential outputs to be shorted to ground.

Under-Voltage Lockout (UVLO)

The SGM4703 incorporates circuitry to detect a low supply voltage for safe and reliable operation. When the supply voltage is first applied, the SGM4703 will remain inactive until the supply voltage exceeds 4.6V (V_{UVLOUP}). When the supply voltage is removed and drops below 4.3V (V_{UVLODN}), the SGM4703 enters into mute mode, where the differential audio outputs VOPL/R and VONL/R are pulled to ground through on-chip resistors (5kΩ) individually.

Over-Voltage Protection (OVP)

The SGM4703 features over-voltage protection. When the supply voltage exceeds 28V (V_{OVPUP}), the device enters into mute mode, where the differential audio outputs VOPL/R and VONL/R are pulled to ground through on-chip resistors (5kΩ) individually. The device will resume normal operation once the supply voltage returns to a value lower than 26.5V (V_{OVPDN}).

Over-Temperature Shutdown (OTSD)

When the die temperature exceeds +160℃, the device enters into mute mode, where the differential audio outputs VOPL/R and VONL/R are pulled to ground through on-chip resistors (5kΩ) individually. The device will resume normal operation once the die temperature returns to a lower temperature, which is about 20℃ lower than the threshold.

DC-Detect Protection (DCP)

The SGM4703 features DCP circuit to protect the speakers from large DC current. A DC-detect fault is issued when the duty cycle of differential outputs of either channel exceeds 20% for more than 720ms at the same polarity. The device enters into mute mode, where the differential audio outputs VOPL/R and VONL/R are pulled to ground through on-chip resistors (5kΩ) individually. Note that the DCP threshold is a function of the supply voltage, as shown in Table 8. To avoid nuisance faults due to the DCP circuit, it is recommended to hold the EN pin low during startup until the audio signals at the inputs are stable. Also, take care to closely match the impedance seen at two differential inputs.

A DC-detect fault is latched and reported on the FAULTB pin as a low state. Also, the SGM4703 enters into mute mode and remains in mute mode. The latch can be cleared by cycling the EN pin through the low state.

Over-Current Protection (OCP)

In operation, the outputs of Class-D amplifiers are constantly monitors for any over-current and/or short-circuit conditions. When a short-circuit condition between two differential outputs, differential outputs to PVDD or ground is detected, the device enters into mute mode, where the differential audio outputs VOPL/R and VONL/R are pulled to ground through on-chip resistors (5kΩ) individually. If the fault persists over a prescribed period, the fault condition is latched and reported on the FAULTB pin as a low state. Also, the SGM4703 enters into mute mode and remains in mute mode. The latch can be cleared by cycling the EN pin through the low state.

If automatic recovery from the OCP fault is desired, connect the FAULTZ pin directly to the EN pin, as shown in Figure 13. It allows the FAULTZ pin to automatically drive the EN pin low, which clears the OCP latch.

Table 7. Protection Modes of Various Operating faults

Fault	Detection Condition	FAULTB	Audio Outputs	Mode	Latched or Self-Recovery
Over-Current	Audio outputs shorted to PVDD or GND or each other	Low	5kΩ to GND	Mute	Latched
DC-Detect	See Table 8	Low	5kΩ to GND	Mute	Latched
Over-Temperature	T_J > 160℃	-	5kΩ to GND	Mute	Self-Recovery
Under-Voltage	PVDD < 4.3V	-	5kΩ to GND	Mute	Self-Recovery
Over-Voltage	PVDD > 28V	-	5kΩ to GND	Mute	Self-Recovery

APPLICATION INFORMATION (continued)

Table 8. DC-Detect Threshold Voltages

PVDD (V)	Output Offset Voltage V_{OS} (V)
6.5	1.3
12	2.4
15	3.0
18	3.6

If automatic recovery from the DCP fault is desired, connect the FAULTB pin directly to the EN pin, as shown in Figure 13. It allows the FAULTB pin to automatically drive the EN pin low, which clears the DCP latch.

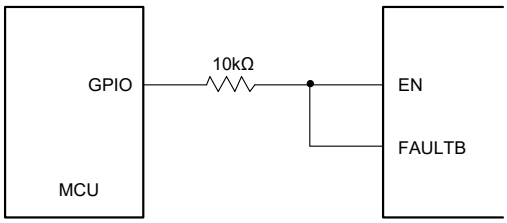


Figure 13. Automatic Recovery from OCP or DCP Fault Latch

Class-D Audio Amplifier

The audio power amplifiers in SGM4703 operate in much the same way as traditional Class-D amplifiers and similarly offer much higher power efficiency.

Fully Differential Amplifier

The SGM4703 includes a pair of fully differential amplifiers with differential inputs and outputs. The fully differential amplifiers ensure that the differential output voltages are equal to the differential input voltages times the amplifier gain. Although the SGM4703 supports for a single-ended input, differential inputs are much preferred for applications where the environment can be noisy in order to ensure maximum SNR.

Low-EMI Filterless Output Stage

Traditional Class-D audio amplifiers require for the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. The SGM4703 applies an edge-rate control circuitry to reduce EMI emissions, while maintaining high power efficiency.

Filterless Design

The SGM4703 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. By eliminating the output filter, a smaller, less costly, and more efficient solution can be accomplished.

Because the frequency of the audio outputs is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum performance, use speakers with series inductances greater than 10μH. Typical 4Ω speakers exhibit series inductances from 10μH to 47μH.

Ferrite Bead Output Filter

With an edge-rate control circuitry in SGM4703, it is possible to design a low EMI, highly efficient Class-D audio amplifier without the need for classic LC reconstruction filters when the amplifier drives speaker loads with short speaker wires (less than 10cm). However, EMI suppression can be further reduced by use of a low-cost ferrite bead filter comprising a ferrite bead and a capacitor, as shown in Figure 14. The ferrite bead filter is applied to block radiation in the range of 30MHz and above from appearing on the speaker wires and the power supply lines. The impedance of the ferrite bead is used with a small capacitor in the range of 1nF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead filter should be less than 10MHz.

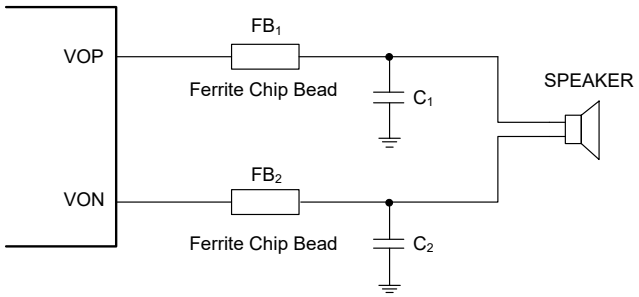


Figure 14. Ferrite Bead Filter for EMI Reduction

Choose a ferrite bead with low DC resistance (DCR) and high impedance (100Ω ~ 330Ω) at high frequencies (>100MHz). The current flowing through the ferrite bead must be also taken into consideration. The effectiveness of ferrites can be greatly aggravated at much lower than their rated current values. Choose a ferrite bead with a rated current no less than 4A for 8Ω loads, 7A for 4Ω loads, and 9A for 3Ω loads (in PBTL configuration).

APPLICATION INFORMATION (continued)

A high quality ceramic capacitor is needed for the ferrite bead filter. A low ESR ceramic capacitor with good temperature and voltage characteristics will be the best choice. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. It is crucial to place each ferrite bead filter tightly together and individually close to VOPL/R and VONL/R pins respectively.

Additional EMI improvements may be obtained by adding snubber networks from each of the Class-D outputs to ground. Suggested values for a simple RC series snubber network are 10Ω in series with a 680pF capacitor. Note that design of the RC snubber circuit is specific to every application and must take into account the parasitic reactance of the system board to reach proper values of R and C. Evaluate and ensure that the voltage spikes (overshoots and undershoots) at VOPL/R and VONL/R on the actual system board are within their absolute maximum ratings. Pay close attention to the layout of the RC snubber circuit to be tight and individually close to VOPL/R and VONL/R pins, respectively.

LC Output Filter

For applications with nearby highly noise sensitive circuits or long speaker wires, it may become necessary to add an LC reconstruction filter for best EMI reduction. A classic second-order low-pass filter, as shown in Figure 15, can be used for the output filter.

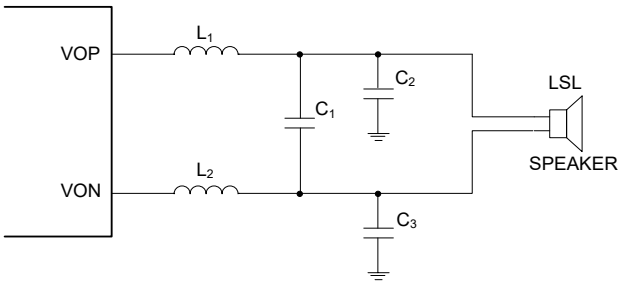


Figure 15. LC Output Filter for EMI Reduction

In Figure 15, the corner frequency of the LC low-pass filter, as given by Equation 3, must be designed to be sufficiently high to allow for high-frequency components of audio signals, yet be low enough to sufficiently attenuate high-frequency components of the audio outputs from VOPL/R and VONL/R. The corner frequency of the filter is typically set about 50kHz. In Equation 3, it is assumed that $L = L_1 = L_2$, $C_G = C_2 = C_3$, and $C = 2 \times C_1 + C_G$.

$$f_{C,\,LPF} = \frac{1}{2\pi\sqrt{LC}} \quad (3)$$

The quality factor Q of the output filter is important. Lower Q increases output noise and higher Q results in passband peaking at frequencies near the corner frequency. The quality factor of the filter is typically set between 0.5 and 0.8. As shown in Equation 4, the speak load, R_{LOAD}, affects the quality factor of the filter.

$$Q = \frac{R_{LOAD}}{2} \times \sqrt{\frac{C}{L}} \quad (4)$$

Table 9 lists suggested component values of L_1, L_2, C_1, C_2, and C_3 for the second-order Butterworth low-pass filter with the speaker load at 2Ω, 3Ω, 4Ω, or 8Ω.

Table 9. Suggested Component Values of LC Output Filter

Speaker Load (Ω)	Modulation Schemes	L_1, L_2 (μH)	C_1 (μF)	C_2, C_3 (μF)	$f_{C,\,LPF}$ (kHz)	Q
8	SSM	15	0.22	0.1	56	0.76
	DSM	15	-	0.56	55	0.77
4	SSM	10	0.47	0.15	48	0.68
	DSM	10	-	1.0	50	0.63
3	SSM	8.2	0.47	0.22	52	0.56
	DSM	8.2	-	1.2	51	0.57
2	SSM	5.6	0.68	0.22	54	0.53
	DSM	5.6	-	1.5	55	0.52

APPLICATION INFORMATION (continued)

Audio Input Capacitors (C_{INL1}, C_{INL2}, C_{INR1} and C_{INR2})

The input DC decoupling capacitors are recommended to bias the incoming audio inputs to a proper DC level. The input capacitor C_{IN}, in conjunction with the amplifier input resistance (including both internal resistor R_{INI} and external resistor R_{INE}, if any) forms a high-pass filter that removes the DC bias of the audio inputs. The corner frequency $f_{C,HPF}$ of the high-pass filter is given by Equation 5. In the equation, it is assumed that R_{INE} = R_{INL1} = R_{INL2} = R_{INR1} = R_{INR2} and C_{IN} = C_{INL1} = C_{INL2} = C_{INR1} = C_{INR2}.

$$f_{C,\,HPF} = \frac{1}{2\pi \times (R_{INE} + R_{INI}) \times C_{IN}} \quad (5)$$

R_{INE} is the external input resistance for a specific voltage gain. Note that the variation of the actual input resistance will affect the voltage gain proportionally. Choose R_{INE} with a tolerance of 2% or better.

Choose C_{IN} such that $f_{C,HPF}$ is well below the lowest frequency of interest. Setting it too high affects the amplifiers' low-frequency response. Consider an example where the specification calls for A_V = 26dB and $f_{C,HPF}$ = 5Hz. In this example, R_{INE} = 0Ω and R_{INI} = 30kΩ and C_{IN} is calculated to be about 1.06μF; thus 1μF, as a common choice of capacitance, can be chosen for C_{IN}.

Any mismatch in capacitance between two audio inputs will cause a mismatch in the corner frequencies. Severe mismatch may also cause turn-on pop noise, PSRR, CMRR performance. Choose C_{IN} with a tolerance of ±2% or better.

Furthermore, the type of the input capacitor is crucial to audio quality. For best audio quality, use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

Supply Coupling Capacitors (C_{PVDD}, C_{AVDD}, C_{GVDD} and C_{PLIMIT})

Decouple each pair of PVDD pins respectively with a 1μF low-ESR ceramic capacitor (X7R or X5R) to GND. It is highly suggested to add an additional 0.01μF ceramic capacitor, in tandem with each 1μF capacitor, for high-frequency decoupling. The rated voltage of the supply coupling capacitors must be higher than the power supply voltage with sufficient tolerance to limit the effects of DC bias. Place the decoupling capacitors as individually close as possible to each pair of PVDD pins.

If the power supply input is located more than a few inches from SGM4703, additional bulk supply decoupling capacitors (electrolytic or tantalum type) may be required. Add a large (220μF or greater) bulk capacitor on the PVDD power bus in close proximity to the SGM4703.

Decouple the AVDD pin with a 1μF low-ESR ceramic capacitor to AGND. Place the decoupling capacitor as close as possible to the AVDD pin. Furthermore, add a small decoupling resistor (R_{AVDD}) of 10Ω between the system power supply and the AVDD pin, preventing high-frequency transients of PVDD from interfering with on-chip linear amplifiers.

Decouple the GVDD pin with a 1μF low-ESR ceramic capacitor to AGND. Place the decoupling capacitor close to the GVDD pin.

Decouple the PLIMIT pin with a 0.1μF low-ESR ceramic capacitor to AGND for high-frequency filtering. Place the decoupling capacitor close to the PLIMIT pin.

PCB LAYOUT

As a high power, high efficiency, Class-D stereo audio power amplifier, the SGM4703 requires proper PCB layout and grounding to ensure high efficiency, low distortion, and low EMI emission. Use wide traces for the power supply inputs (PVDD) and audio outputs (VOPL/R and VONL/R) to minimize losses due to parasitic trace resistances. Route all traces that carry switching transients away from the traces or components in the audio signal path.

Ground Plane – It is required to use a solid metal plane with sufficiently wide area as a central ground GND for SGM4703. All the power ground pins PGND are directly shorted to the large ground plane GND, which serves as a central “star” ground for the SGM4703. Use a single point of connection between the analog ground AGND and the ground plane GND to minimize the coupling of high-current switching noise onto audio signals.

Supply Decoupling Capacitors – The supply decoupling capacitors (C_{PVDD} and C_{AVDD}) should be placed as individually close as possible to PVDD and AVDD pins.

Output Filters – Place each audio output filter (ferrite bead or LC filter) individually close to their respective output pins, VOPL/R and VONL/R, for best EMI performance and operational robustness. Keep the current loop from each of the audio outputs through the output filters and back to the PGND pins as short and tight as possible.

Power Dissipation – The maximum output power of SGM4703 can be severely limited by its thermal dissipation capability. To ensure the device operating properly and reliably at maximum output power without incurring over-temperature shutdown, the following guidelines are given for best thermal dissipation capability:

- Fill both top and bottom layers of the system board with solid GND metal traces.
- Solder the thermal pad directly onto a grounded metal plane.
- Place lots of equally-spaced vias underneath the thermal pad connecting the top and bottom layers of GND. The vias are connected to a solid metal plane on the bottom layer of the board.
- Reserve wide and uninterrupted areas along the thermal flow on the top layer, i.e., no wires cutting through the GND layer and obstructing the thermal flow.
- Avoid using vias for traces carrying high current.

TYPICAL APPLICATION CIRCUITS

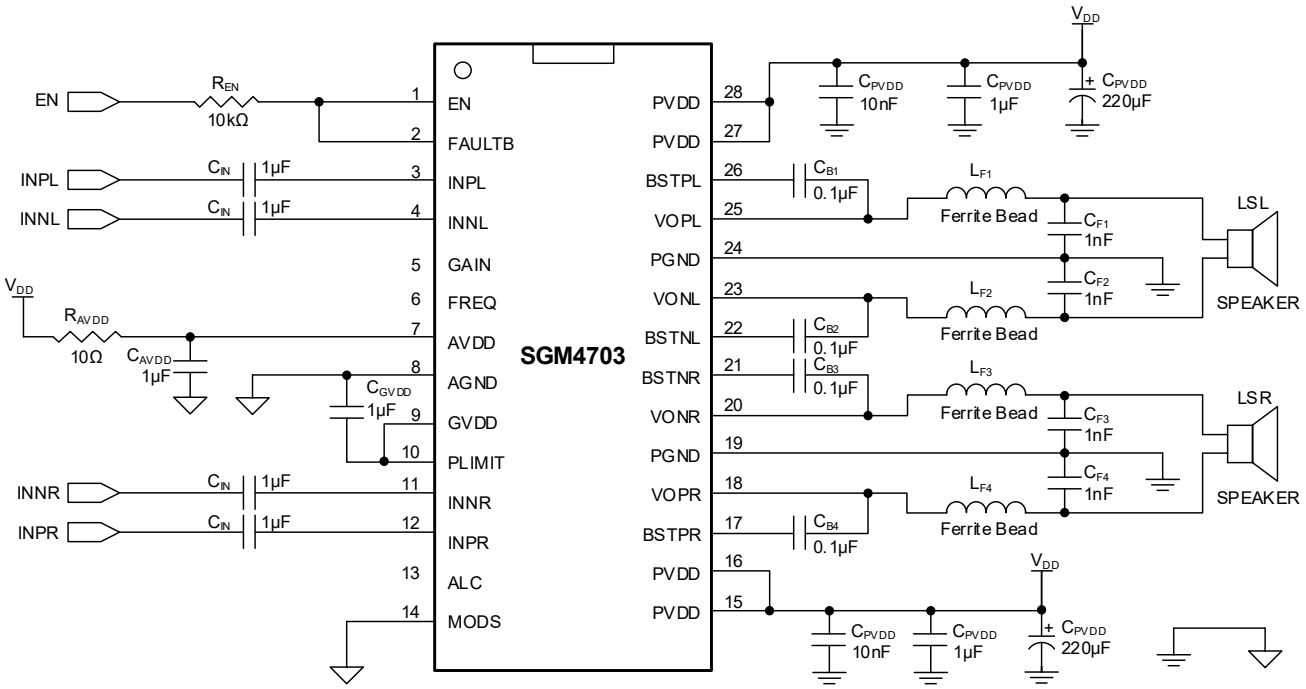


Figure 16. Differential Inputs in Non-ALC Mode with DSM

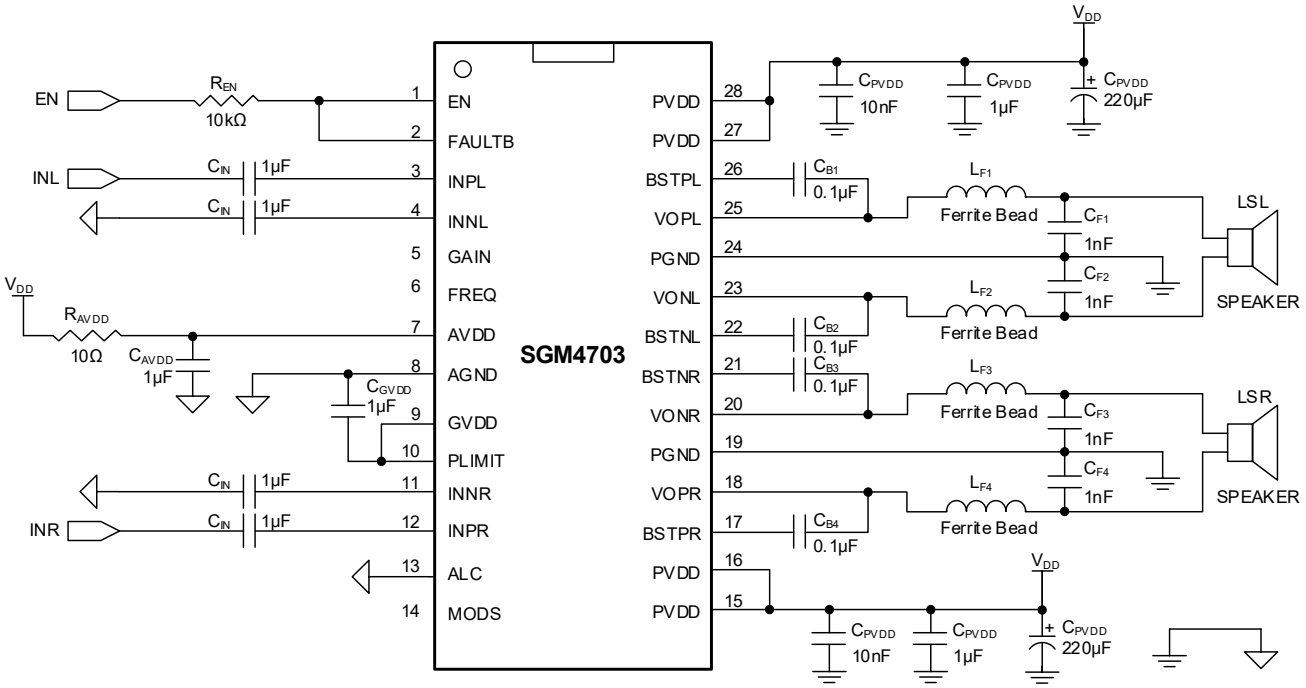


Figure 17. Single-Ended Inputs in ALC-1 Mode with SSM

TYPICAL APPLICATION CIRCUITS (continued)

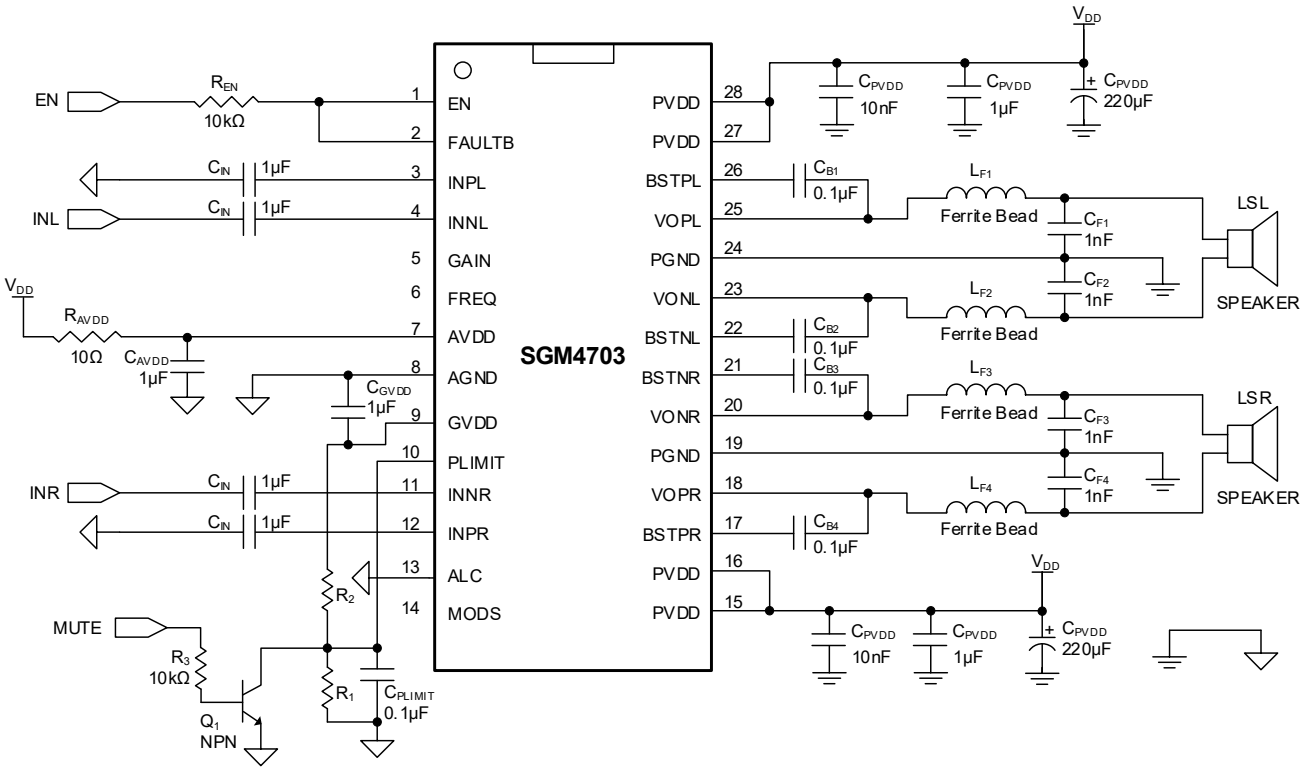


Figure 18. Single-Ended Inputs in APL Mode with Mute Control

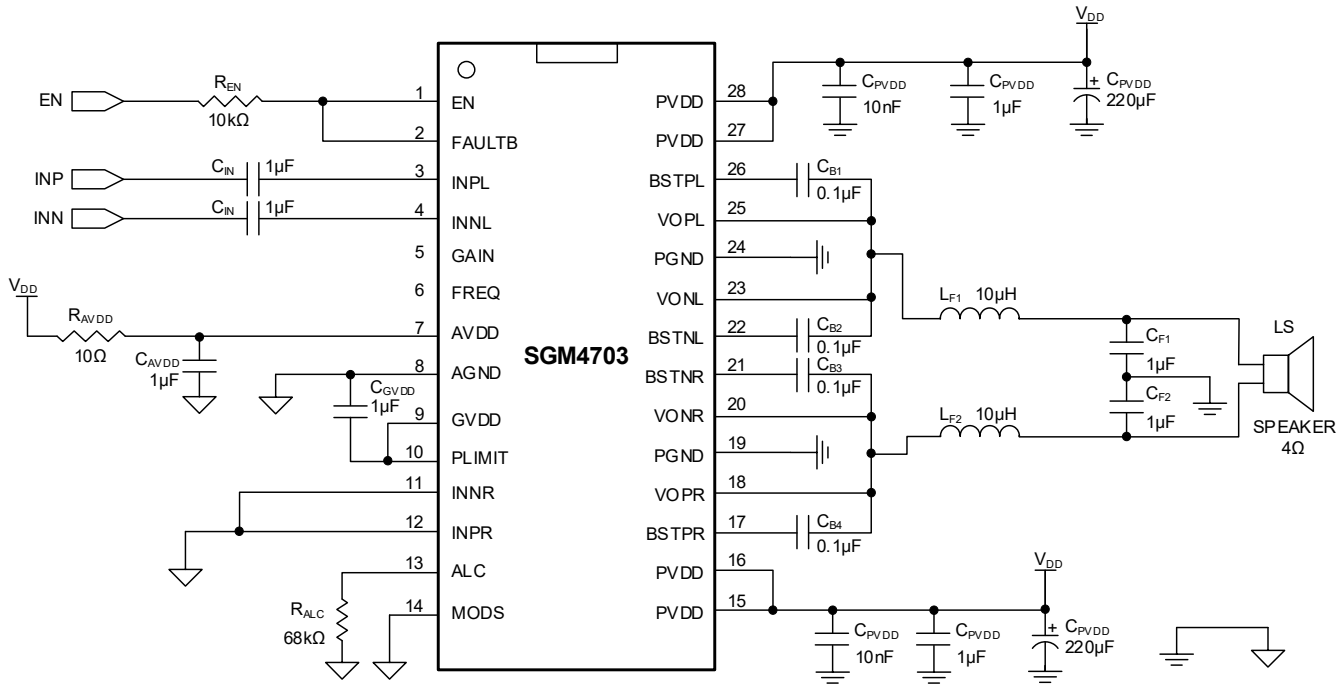


Figure 19. Differential Inputs in ALC-2 Mode with DSM in PBTL Configuration

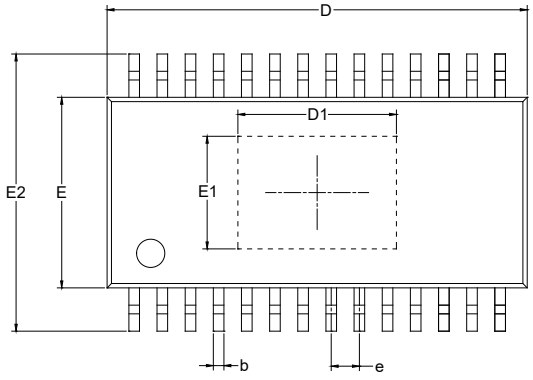
REVISION HISTORY

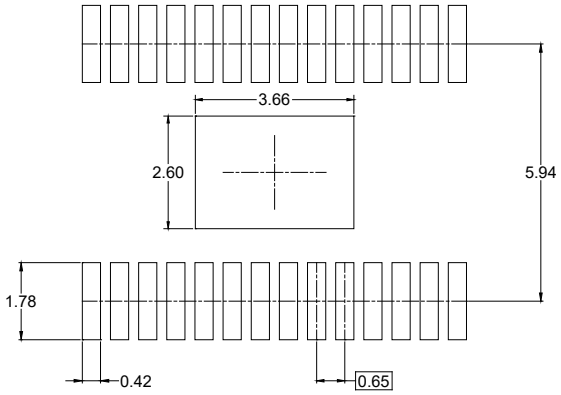
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

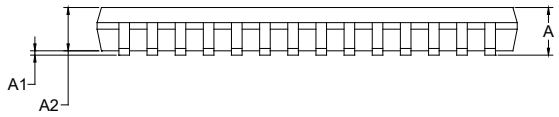
PACKAGE OUTLINE DIMENSIONS

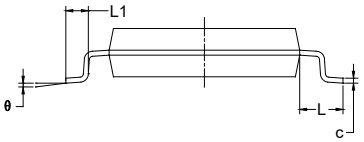
TSSOP-28 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)





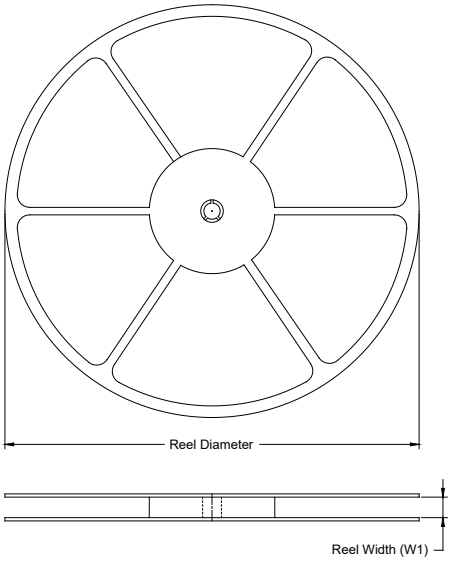
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
D1	3.460	3.860	0.136	0.152
E	4.300	4.500	0.169	0.177
E1	2.400	2.800	0.094	0.110
E2	6.200	6.600	0.244	0.260
e	0.650 BSC		0.026 BSC	
L	1.000 BSC		0.039 BSC	
L1	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

NOTES:

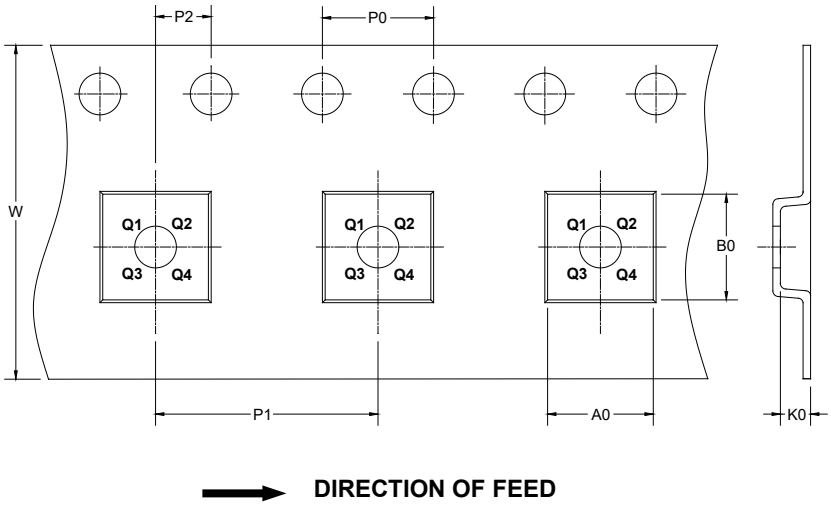
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

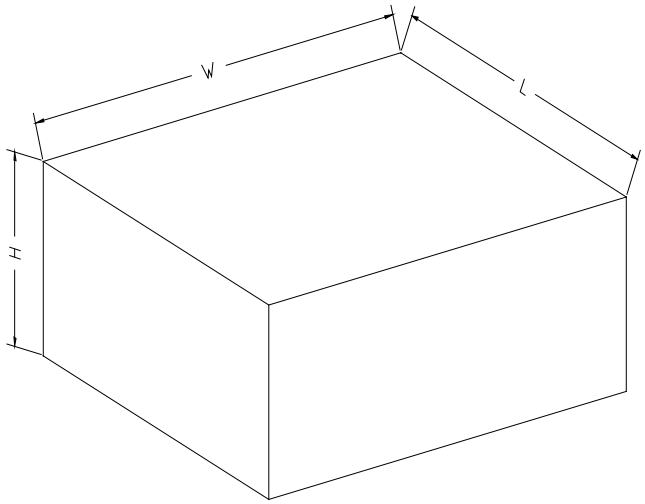
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-28 (Exposed Pad)	13″	17.6	6.80	10.20	1.60	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002