OP07x 精密运算放大器

1 特性

- 低噪声
- 无需外部元件
- 以更低的成本更换斩波放大器
- 宽输入电压范围：
  0V 至 ±14V（典型值，±15V 电源）
- 宽电源电压范围：±3V 至 ±18V

2 应用

- 模拟输入模块
- 电池测试
- 实验室和现场仪表
- 温度变送器
- 商用网络和服务器 PSU

3 说明

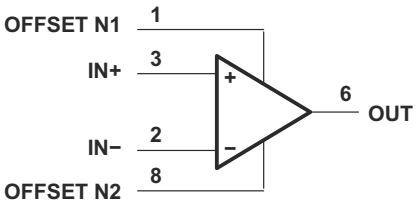
通过低噪声、无斩波、双极输入晶体管放大器电路，OP07C 和 OP07D (OP07x) 器件可提供低失调电压和长期稳定性。对于大多数应用，无需外部元件即可实现失调电压归零和频率补偿。真差分输入连同宽输入电压范围和出色的共模抑制能力，有助于在高噪声环境和同相应用中提供出色的灵活性和性能。在整个温度范围内，该类器件可维持低偏置电流和超高的输入阻抗。

要获得更高的性能和更宽的温度范围，请参阅下一代具有低功耗的 OPA207 和具有重容性负载驱动能力的 OPA202。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
OP07C、OP07D	D（SOIC，8）	4.90mm × 3.91mm
	P（PDIP，8）	9.81mm × 6.35mm
	PS（SO，8）	6.20mm × 5.30mm

(1) 如需了解所有可用封装和 OP07，请参阅数据表末尾的可订购产品附录。



简化版原理图

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (November 2014) to Revision H (July 2022) — **Page**

- 向宽输入电压范围特性要点添加了电源条件 1
- Changed VCC_+ to V+ and VCC_- to V− 3
- Changed supply voltage abbreviation from VCC+ and VCC – to V_S in *Absolute Maximum Ratings* and throughout the data sheet 4
- Changed note 5 in *Absolute Maximum Ratings* to include a note that fast-ramping shorts to the positive supply can damage the device 4
- Changed Electrostatic discharge Human-body model and Charged-device model from 1000 V to ±1000 V 4
- Added new values to *Thermal Information* 4
- Changed *Electrical Characteristics* format 5
- Changed parameter name from supply-voltage sensitivity to power supply rejection ratio in *Electrical Characteristics* 5
- Changed parameter name from input offset voltage to Input voltage noise density in *Electrical Characteristics* 5
- Changed input current noise density unit from nV/ √ Hz to pA/ √ Hz in *Electrical Characteristics* 5
- Changed parameter name from large-signal differential voltage gain to open-loop voltage gain in *Electrical Characteristics* 5
- Changed parameter name from peak output voltage to voltage output swing in Electrical Characteristics 5
- Changed functional block diagram 8
- Changed text to clarify how to adjust input mismatches using null pins in *Application Information* 9

Changes from Revision F (January 2014) to Revision G (November 2014) — **Page**

- 添加了 *应用*、*器件信息* 表、*引脚功能* 表、*处理等级* 表、*热性能信息* 表、*典型特性*、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分 1

Changes from Revision E (May 2004) to Revision F (January 2014) — **Page**

- 删除了 *订购信息* 表 1

5 Pin Configuration and Functions

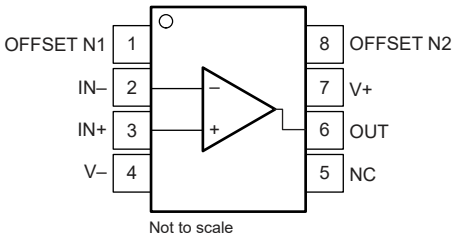


图 5-1. D Package, 8-Pin SOIC, P Package, 8-Pin PDIP, and PS Package, 8-Pin SO (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN+	3	Input	Noninverting input
IN –	2	Input	Inverting input
NC	5	—	Do not connect
OFFSET N1	1	Input	External input offset voltage adjustment
OFFSET N2	8	Input	External input offset voltage adjustment
OUT	6	Output	Output
V+	7	—	Positive supply
V –	4	—	Negative supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_S	Supply voltage((2))	Single supply		44	V
		Dual supply		±22	
	Input voltage	Differential(3)		±30	V
		Single-ended(4)		±22	
	Output short-circuit(5)		Continous		
T_J	Operating junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the midpoint between V+ and V−.
(3) Differential voltages are at IN+ with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output can be shorted to ground or to the negative power supply. Fast ramping shorts to the positive supply can cause permanent damage and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single supply	6		36	V
		Dual supply	±3		±18	
V_{CM}	Common-mode input voltage	V_S = ±15 V	–13		13	V
T_A	Operating ambient temperature		0		70	°C

6.4 Thermal Information

THERMAL METRIC(1)		OP07x		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.6	85	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.1	68.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.4	55..6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.7	38.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.6	55.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 2 kΩ connected to mid-supply, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)(1).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OP07C			±60		µV
			T_A = 0°C to 70°C		±85		
		OP07D				±150	
			T_A = 0°C to 70°C			±250	
dV_{OS}/dT	Input offset voltage drift	T_A = 0°C to 70°C	OP07C		±0.5		µV/°C
			OP07D			±2.5	
	Long-term drift of input offset voltage(2)				±0.4		µV/mo
	Offset adjustment range	R_s = 20 kΩ, see 节 8.1			±4		mV
PSRR	Power supply rejection ratio	V_S = ±3 V to ±18 V			7	32	µV/V
			T_A = 0°C to 70°C		10	51	
INPUT BIAS CURRENT							
I_B	Input bias current	OP07C			±1.8		nA
			T_A = 0°C to 70°C		±2.2		
		OP07D				±12	
			T_A = 0°C to 70°C			±14	
	Input bias current drift	OP07C			±18		pA/°C
		OP07D				±50	
I_{OS}	Input offset current	OP07C			±0.8		nA
			T_A = 0°C to 70°C		±1.6		
		OP07D				±6	
			T_A = 0°C to 70°C			±8	
	Input offset current drift	OP07C			12		pA/°C
		OP07D				±50	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			0.38		μV_{PP}
e_N	Input voltage noise density	f = 10 Hz			10.5		nV/√Hz
		f = 100 Hz			10.2		
		f = 1 kHz			9.8		
	Input current noise	f = 0.1 Hz to 10 Hz			15		pA_{pp}
i_N	Input current noise density	f = 10 Hz			0.35		pA/√Hz
		f = 100 Hz			0.15		
		f = 1 kHz			0.13		
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage			±13	±14		V
		T_A = 0°C to 70°C		±13	±13.5		
CMRR	Common-mode rejection ratio	OP07C V_{CM} = ±13 V		100	120		dB
			T_A = 0°C to 70°C	97	120		
		OP07D V_{CM} = ±13 V		94	110		
			T_A = 0°C to 70°C	94	106		
INPUT CAPACITANCE							
r_I	Input resistance			7	33		MΩ
OPEN-LOOP GAIN							

6.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 2 kΩ connected to mid-supply, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)(1).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_{OL}	Open-loop voltage gain	1.4 V < V_O < 11.4 V, R_L = 500 kΩ	OP07C	100	400		V/mV
			OP07D		400		
		V_O = ±10 V		120	400		
			T_A = –40°C to +125°C	100	400		

6.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 2 kΩ connected to mid-supply, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
	Unity gain bandwidth		0.4	0.6		MHz
SR	Slew rate	V_S = 5 V, R_L = 2 kΩ		0.3		V/ μ s
OUTPUT						
	Voltage output swing		±11.5	±12.8		V
		T_A = 0°C to 70°C	±11	±12.6		
		R_L = 10 kΩ	±12	±13		
		R_L = 1 kΩ		±12		
POWER SUPPLY						
P_D	Power dissipation	No load		80	150	mW
		V_S = ±3 V, no load		4	8	

(1) The specifications listed in the *Electrical Characteristics* apply to OP07C and OP07D.
(2) Because long-term drift cannot be measured on the individual devices before shipment, this specification is not intended to be a warranty. This specification is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first 30 days of operation.

6.6 Typical Characteristics

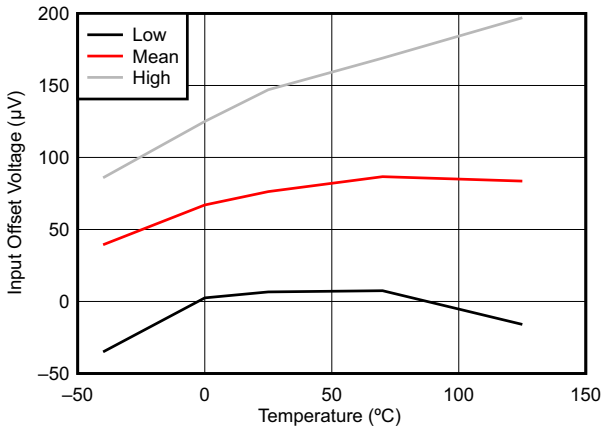


图 6-1. Input-Offset Voltage vs Temperature

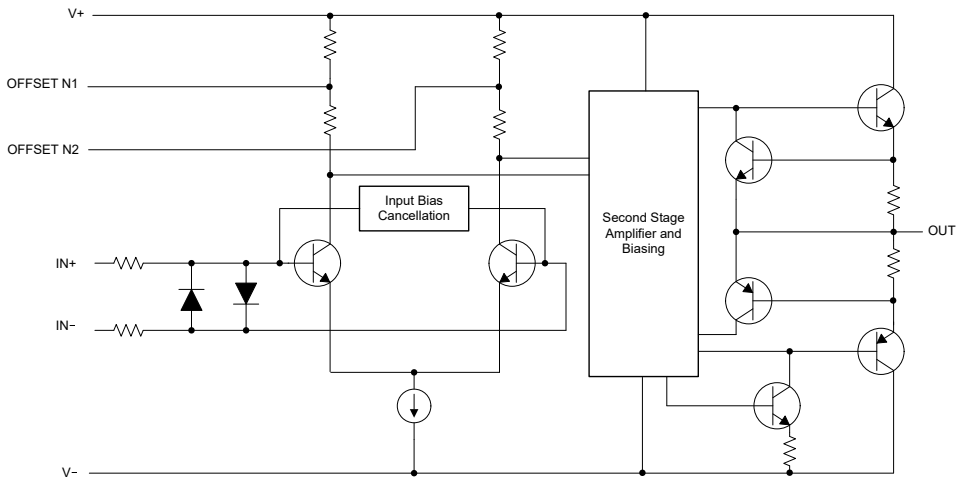
7 Detailed Description

7.1 Overview

These devices offer low offset and long-term stability by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input-voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.

These devices are characterized for operation from 0°C to 70°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Offset-Voltage Null Capability

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors, and so on. The input offset pins allow the designer to adjust for these mismatches by external circuitry. See 节 8 for more details on design techniques.

7.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change the output when there is a change on the input. The OP07x have a 0.3-V/ μ s slew rate.

7.4 Device Functional Modes

The OP07x are powered on when the supply is connected. The devices can be operated as single-supply operational amplifiers or dual-supply amplifiers, depending on the application.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors, and so on. The input offset pins allow the designer to adjust for these mismatches with external circuitry. 图 8-1 shows how these input mismatches can be adjusted by putting resistors or a potentiometer between the null pins. Use a potentiometer to fine tune the circuit during testing or for applications that require precision offset control. For more information about designing using the input-offset pins, see the *Nulling Input Offset Voltage of Operational Amplifiers* application report.

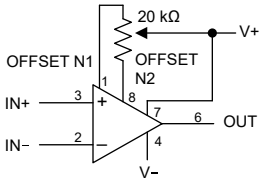


图 8-1. Input Offset-Voltage Null Circuit

8.2 Typical Application

The voltage follower configuration of the operational amplifier is used for applications where a weak signal is used to drive a relatively high current load. This circuit is also called a buffer amplifier or unity gain amplifier. The inputs of an operational amplifier have a very high resistance that puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so the amplifier can provide as much current as necessary to the output load.

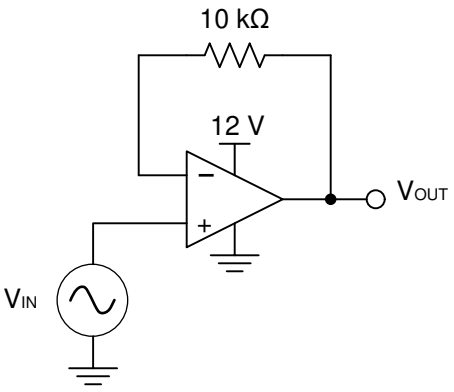


图 8-2. Voltage Follower Schematic

8.2.1 Design Requirements

- Output range of 2 V to 11 V
- Input range of 2 V to 11 V

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Swing

The output voltage of an operational amplifier is limited by the internal circuitry to some level less than the supply rails. For this amplifier, the output voltage swing is within ±12 V, which accommodates the input and output voltage requirements.

8.2.2.2 Supply and Input Voltage

For correct operation of the amplifier, neither input must be higher than the recommended positive supply rail voltage or lower than the recommended negative supply rail voltage. The chosen amplifier must be able to operate at the supply voltage that accommodates the inputs. Because the input for this application goes up to 11 V, the supply voltage must be 12 V. Using a negative voltage on the lower rail, rather than ground, allows the amplifier to maintain linearity for inputs below 2 V.

8.2.3 Application Curves

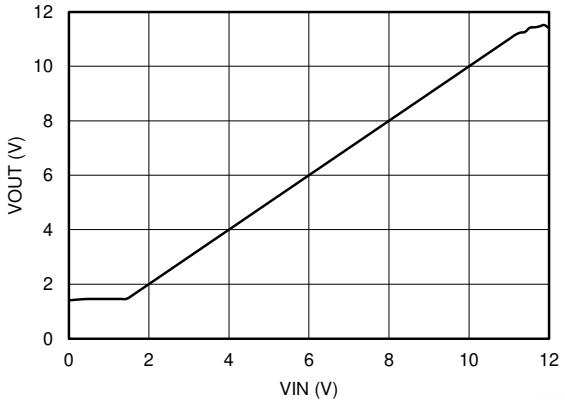


图 8-3. Output Voltage vs Input Voltage

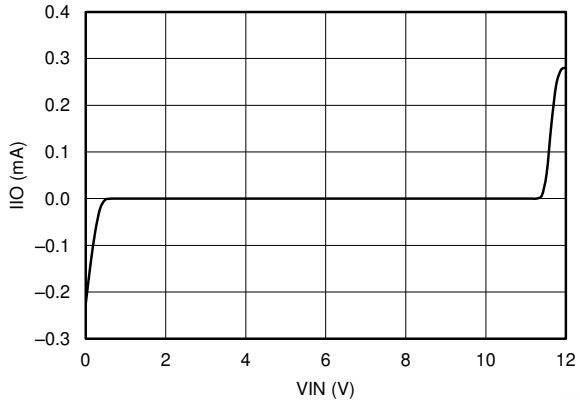


图 8-4. Current Drawn by the Input of the Voltage Follower (I_{IO}) vs Input Voltage

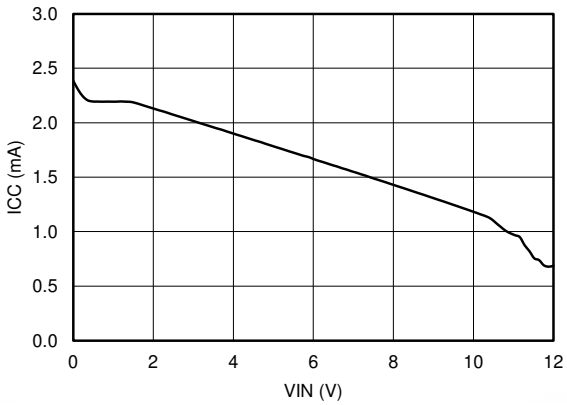


图 8-5. Current Drawn from Supply (I_{CC}) vs Input Voltage

8.3 Power Supply Recommendations

The OP07x operate from ±3 V to ±18 V supplies; many specifications apply from 0°C to 70°C.

CAUTION

Supply voltages larger than ±22 V can permanently damage the device. See also 节 6.1.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more details on bypass capacitor placement, see 节 *8.4.1*.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. On multilayer PCBs, one or more layers are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicularly, as opposed to in parallel, with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in 节 8.4.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

8.4.2 Layout Example

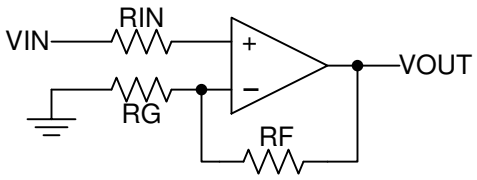


图 8-6. Operational Amplifier Schematic for Noninverting Configuration

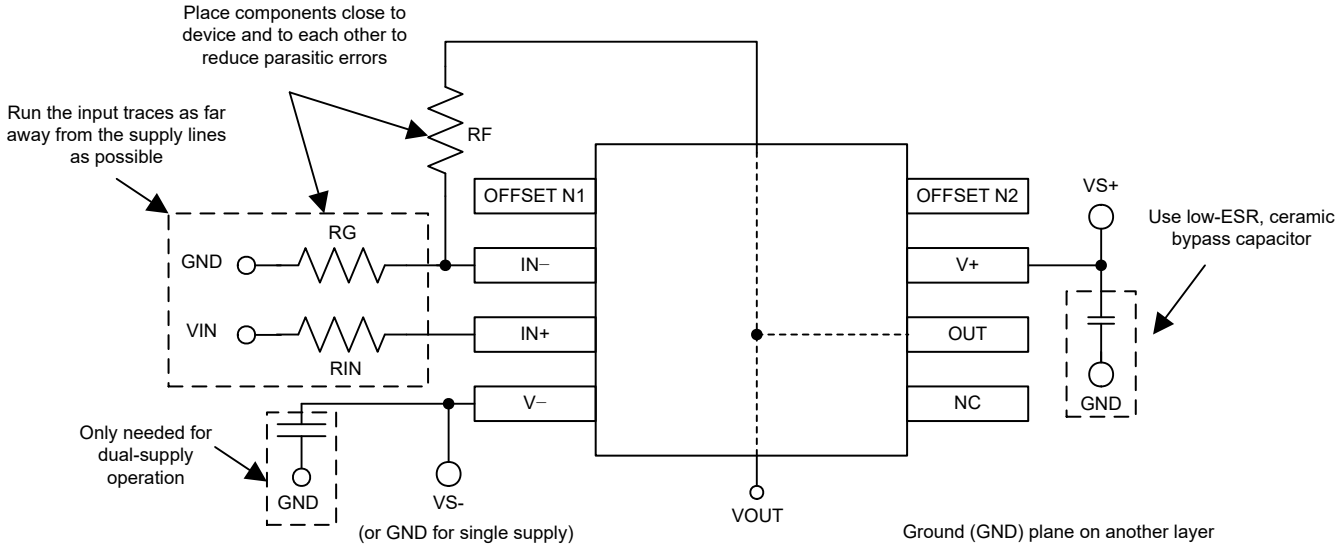


图 8-7. Operational Amplifier Board Layout for Noninverting Configuration

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OP-07DP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	OP-07DP
OP-07DP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	See OP-07DP	OP-07DP
OP-07DPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	OP-07D
OP-07DPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	See OP-07DPS	OP-07D
OP-07DPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	OP-07D
OP-07DPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See OP-07DPSR	OP-07D
OP07CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	OP07C
OP07CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	OP07C
OP07CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See OP07CDR	OP07C
OP07CDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See OP07CDR	OP07C
OP07CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	OP07CP
OP07CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	See OP07CP	OP07CP
OP07CP.B	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	See OP07CP	OP07CP
OP07DD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	OP07D
OP07DD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	See OP07DD	OP07D
OP07DDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	OP07D
OP07DDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See OP07DDR	OP07D
OP07DP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	OP07DP
OP07DP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	See OP07DP	OP07DP
OP07DPE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	OP07DP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

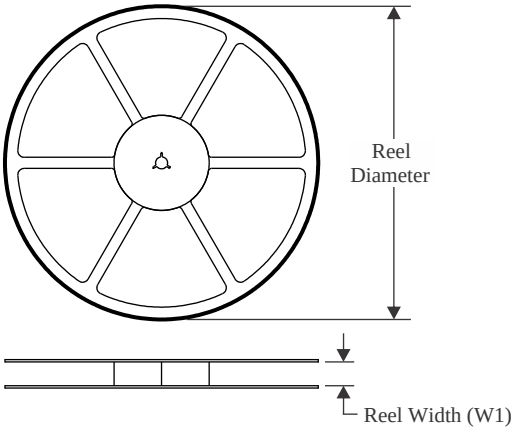
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

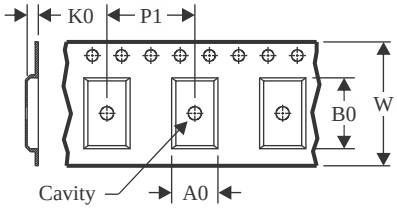
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

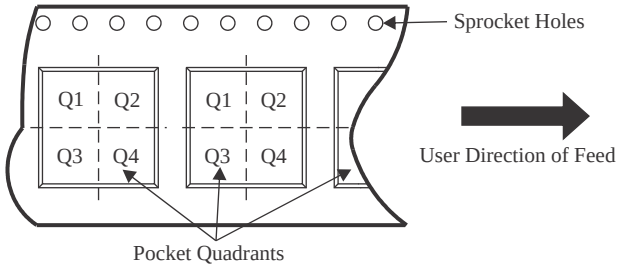


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

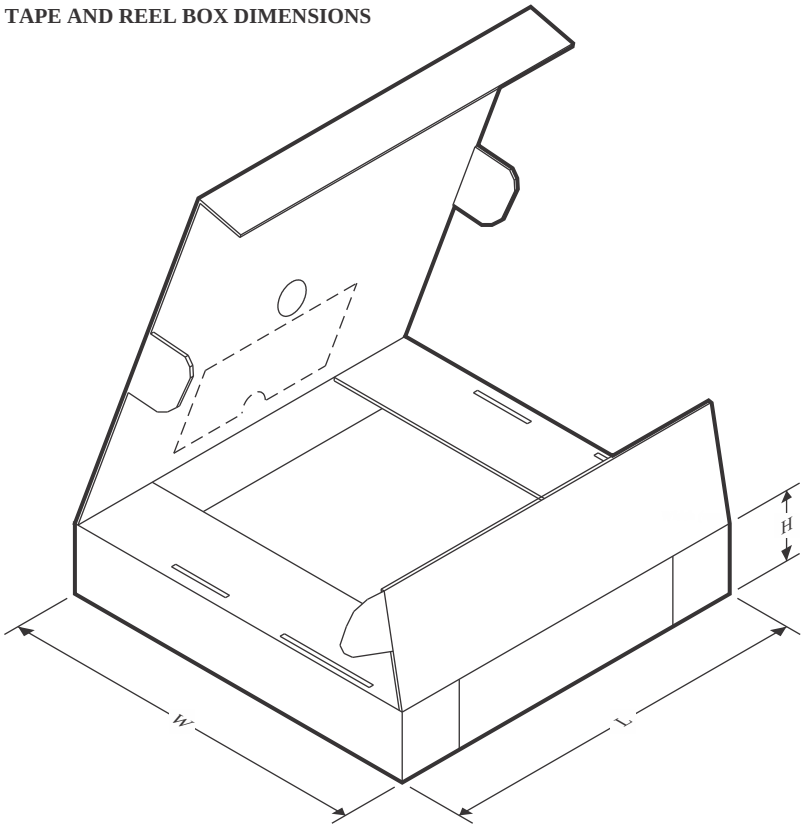
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OP-07DPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
OP07CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OP07CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OP07CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OP07DDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

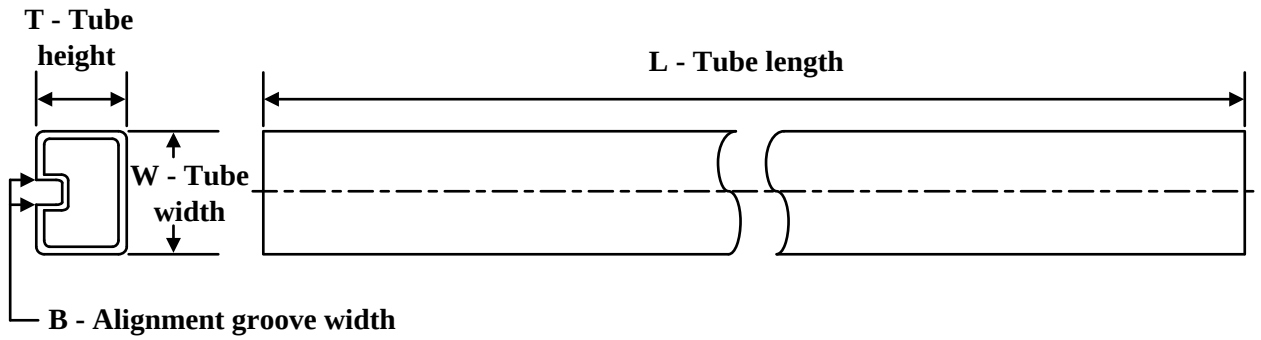
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OP-07DPSR	SO	PS	8	2000	353.0	353.0	32.0
OP07CDR	SOIC	D	8	2500	353.0	353.0	32.0
OP07CDR	SOIC	D	8	2500	340.5	338.1	20.6
OP07CDR	SOIC	D	8	2500	353.0	353.0	32.0
OP07DDR	SOIC	D	8	2500	353.0	353.0	32.0

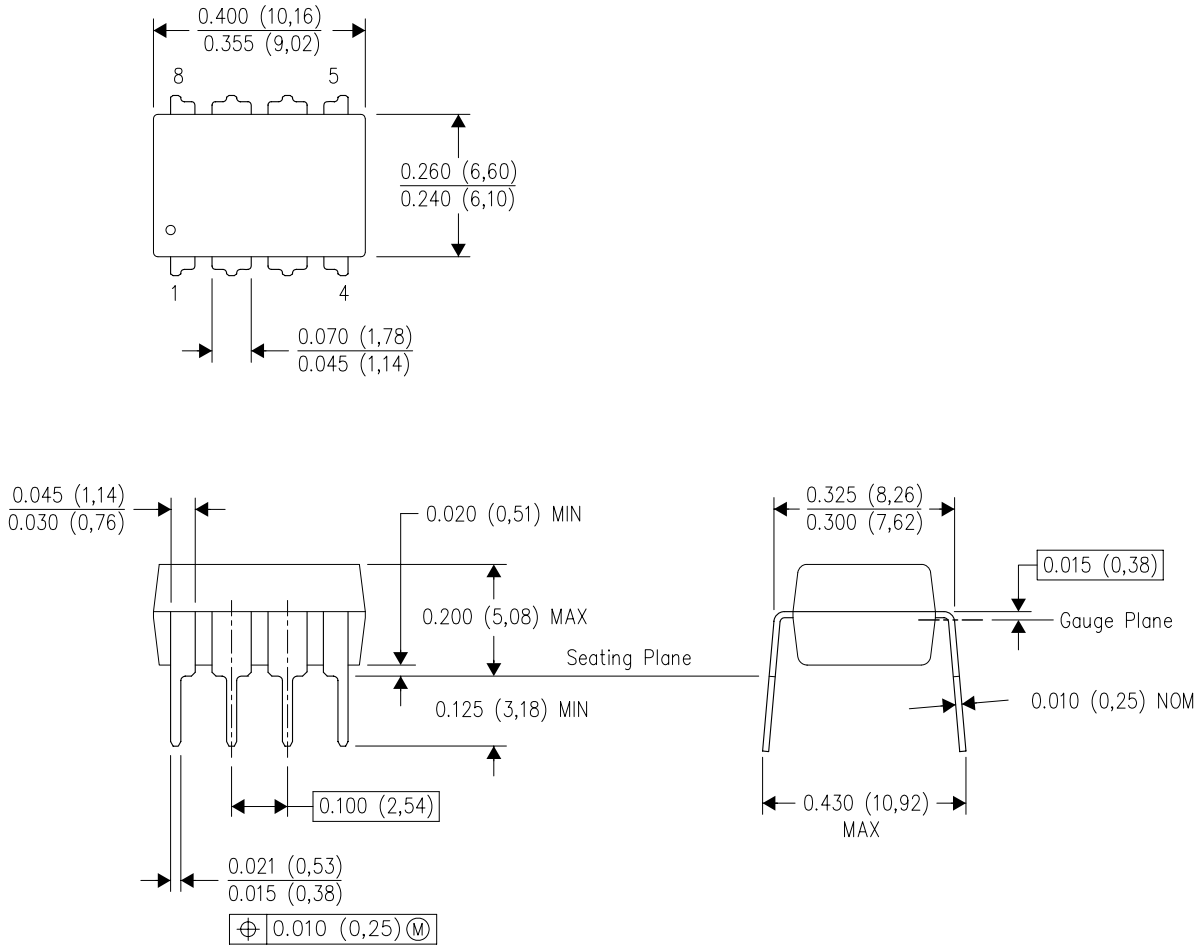
TUBE



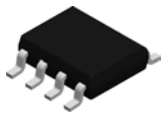
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OP-07DP	P	PDIP	8	50	506	13.97	11230	4.32
OP-07DP.A	P	PDIP	8	50	506	13.97	11230	4.32
OP-07DPS	PS	SOP	8	80	530	10.5	4000	4.1
OP-07DPS.A	PS	SOP	8	80	530	10.5	4000	4.1
OP07CP	P	PDIP	8	50	506	13.97	11230	4.32
OP07CP.A	P	PDIP	8	50	506	13.97	11230	4.32
OP07CP.B	P	PDIP	8	50	506	13.97	11230	4.32
OP07DD	D	SOIC	8	75	507	8	3940	4.32
OP07DD.A	D	SOIC	8	75	507	8	3940	4.32
OP07DP	P	PDIP	8	50	506	13.97	11230	4.32
OP07DP.A	P	PDIP	8	50	506	13.97	11230	4.32
OP07DPE4	P	PDIP	8	50	506	13.97	11230	4.32

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

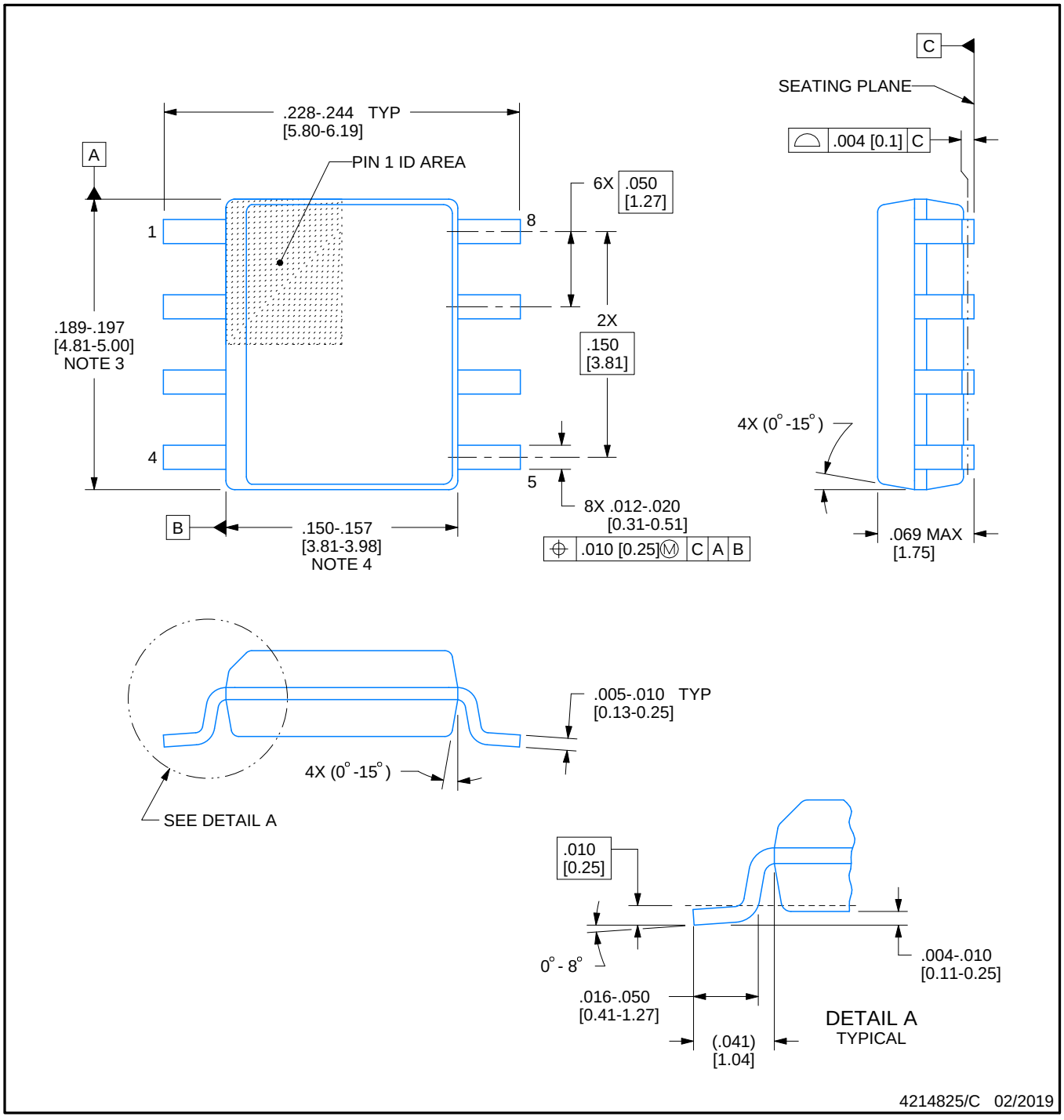


PACKAGE OUTLINE

D0008A

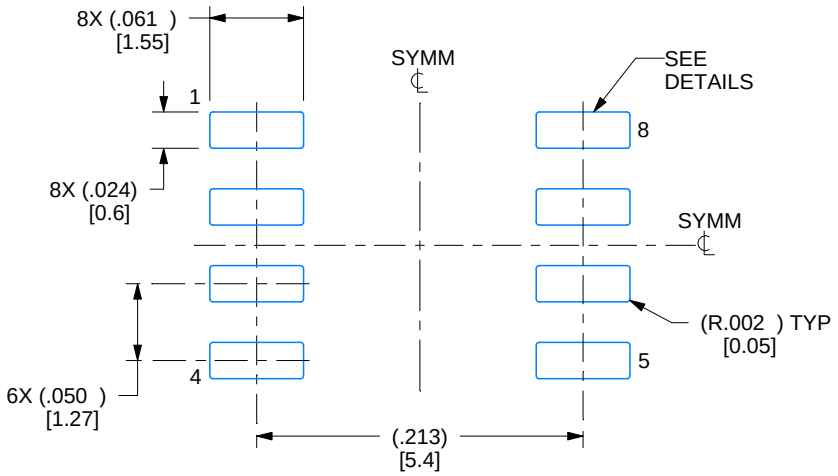
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

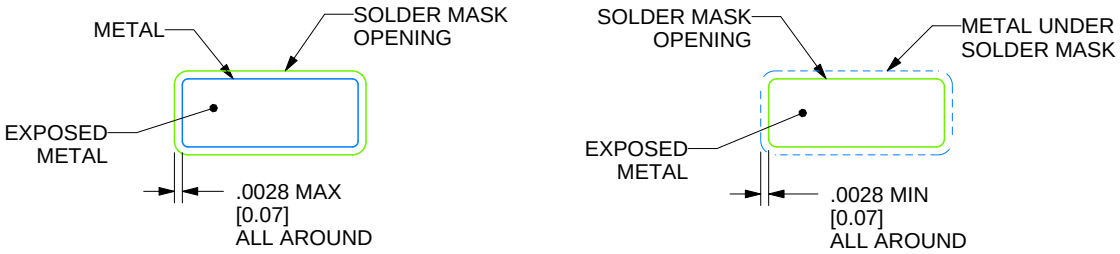


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

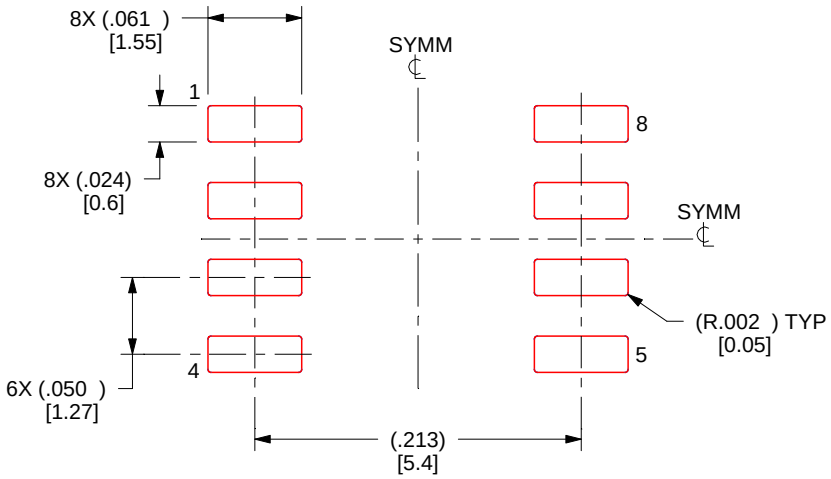
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

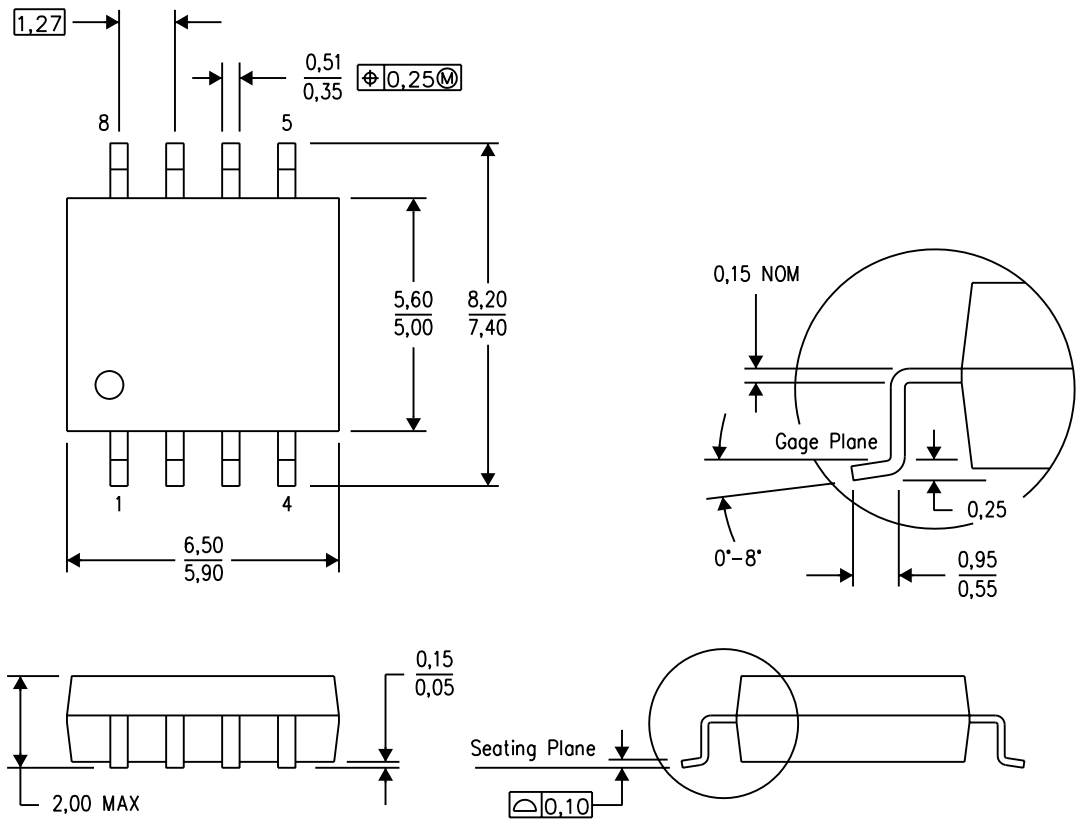
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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