LF411 FET-Input Operational Amplifier

1 Features

- Low input bias current: 50pA typical
- Low input noise current: 2fA/$\sqrt{\text{Hz}}$ typical
- Low supply current: 560µA typical
- High input impedance: $10^{12}\Omega$ typical
- Low total harmonic distortion

2 Applications

- High-speed integrator
- Fast digital-to-analog converter (DAC)
- Sample-and-hold circuit

3 Description

This device is a low-cost, high-speed, FET-Input operational amplifier with very low input offset voltage and a maximum input offset voltage drift. This device requires low supply current, yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage FET input provides very low input bias and offset currents.

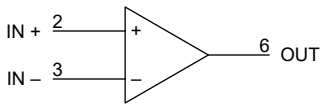
The LF411 is designed for applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF411C is characterized for operation from 0°C to 70°C. The LF411I is characterized for operation from –40°C to +85°C.

Package Information

T_A	V_{IO}max AT 25°C	PACKAGE(1)	
		SMALL OUTLINE (D)(2)	PLASTIC DIP (P)
0°C to 70°C	2mV	LF411CD	LF411CP
–40°C to +85°C	2mV	LF411ID	LF411IP

(1) For more information, see Section 8.
(2) D packages are available taped and reeled. Add the suffix R to the device type (for example, LF411CDR).



Symbol

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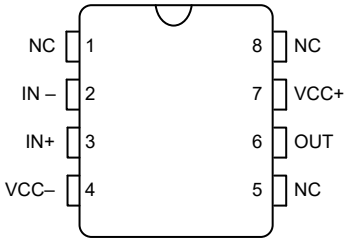
4 Pin Configuration and Functions



Not to Scale

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	NC	—	Do not connect
2	IN–	Input	Input negative
3	IN+	Input	Input positive
4	VCC–	—	Power supply negative
5	NC	—	Do not connect
6	OUT	Output	Output
7	VCC+	—	Power supply positive
8	NC	—	Do not connect

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}+	Supply voltage, positive			18	V
V_{CC}–	Supply voltage, negative			–18	V
V_{ID}	Differential input voltage			±30	V
V_I (1)	Input voltage			±15	V
	Duration of output short circuit		Unlimited		
	Continuous total power dissipation			500	mW
θ_{JA} (2)	Package thermal impedance:	D package		197	°C/W
		P package		104	°C/W
T_{stg}	Storage temperature		–65	+150	°C

(1) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.
(2) The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

5.2 Recommended Operating Conditions

		C SUFFIX		I SUFFIX		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}+	Supply voltage	3.5	18	3.5	18	V
V_{CC}–	Supply voltage	–3.5	–18	–3.5	–18	V
T_A	Operating free-air temperature	0	70	–40	+85	°C

5.3 Electrical Characteristics

over operating free-air temperature range, V_{CC}± = ±15V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A		MIN	TYP	MAX	UNIT
			LF411C	LF411I				
V_{IO}	Input offset voltage	V_{IC} = V_{CM}, R_S = 10kΩ	25°C	25°C		0.8	2	mV
α_{VIO}	Average temperature coefficient of input offset voltage	V_{IC} = 0V, R_S = 10kΩ				10	20	µV/°C
I_{IO}	Input offset current (1)	V_{IC} = 0V	25°C	25°C		25	100	pA
			70°C	85°C			2	nA
I_{IB}	Input bias current (1)	V_{IC} = 0V	25°C	25°C		50	200	pA
			70°C	85°C			4	nA
V_{ICR}	Common-mode input voltage range				±11	−11.5 to 14.5		V
V_{OM}	Maximum peak output-voltage swing	R_L = 10kΩ			±12	±14.95		V
A_{VD}	Large-signal differential voltage	V_{OUT} = ±10V, R_L = 2kΩ	25°C	25°C	25	200		V/mV
			0°C to 70°C	–40°C to +85°C	15	200		
r_i	Input resistance	T_J = 25°C				10^{12}		Ω
CMRR	Common-mode rejection ratio	R_S ≤ 10kΩ			70	100		dB
k_{SVR}	Supply-voltage rejection ratio (2)				70	100		dB
I_{CC}	Supply current					0.56	3.4	mA
SR	Slew rate		25°C	25°C		0.5		V/µs

5.3 Electrical Characteristics (continued)

over operating free-air temperature range, V_{CC}± = ±15V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A		MIN	TYP	MAX	UNIT
			LF411C	LF411I				
B_1	Unity-gain bandwidth		25°C	25°C		4.5		MHz
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω	25°C	25°C		10.8		nV/√Hz
I_n	Equivalent input noise current	f = 1kHz	25°C	25°C		2		fA/√Hz

(1) Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Use pulse techniques that maintain the junction temperatures as close as possible to the ambient temperature.
(2) Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.3 Trademarks

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6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 1997) to Revision D (October 2025)	Page
• Change from JFET to FET	0
• Changed low input noise current from 0.01pA/√Hz to 2fA/√Hz in *Features*	1
• Changed low supply current from 2mA to 560µA in *Features*	1
• Deleted "Low 1/f Noise Corner, 50Hz Typ" from *Features*	1
• Deleted "Package Options Include Plastic Small-Online (D) and Standard (P) DIPs" from *Features*	1
• Changed "JFET-Input operational amplifier with very low input offset voltage" to "FET-Input operational amplifier with very low input offset voltage", and "In addition, the matched high-voltage JFET input provides very low input bias and offset currents" to "In addition, the matched high-voltage FET input provides very low input bias and offset currents" in *Description*	1
• Deleted BAL1 and BAL2 from *Symbol*	1
• Changed pin 1 from BAL1 to NC, and pin 5 from BAL2 to NC	2
• Deleted Lead temperature 1,6mm (1/16inch) from case for 10 seconds row from *Absolute Maximum Ratings*	3
• Updated maximum peak output voltage swing typical value from ±13.5 to ±14.95VUpdated Supply current typical value from 2V to 0.56VUpdated Slew rate, Unity-gain bandwidth, Equivalent input noise voltage, Equivalent input noise current values	3
• Changed input offset voltage test condition from V_{IC}= 0 to V_{IC} = V_{CM} in *Electrical Characteristics*	3

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF411CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	LF411C
LF411CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF411C
LF411CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF411C
LF411CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
LF411CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF411CP
LF411CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF411CP
LF411CPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

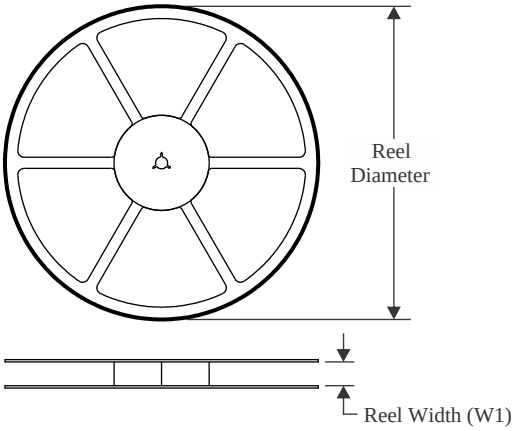
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

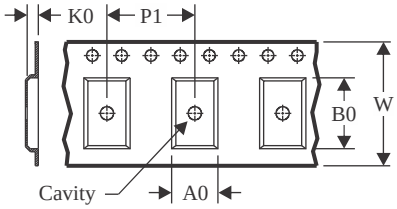
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

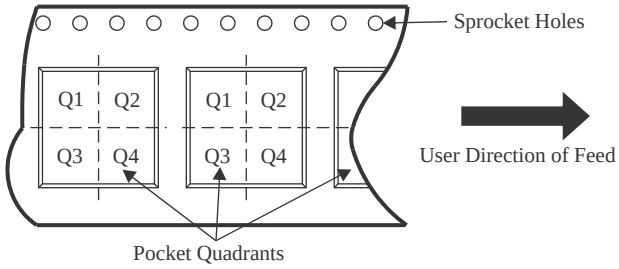


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

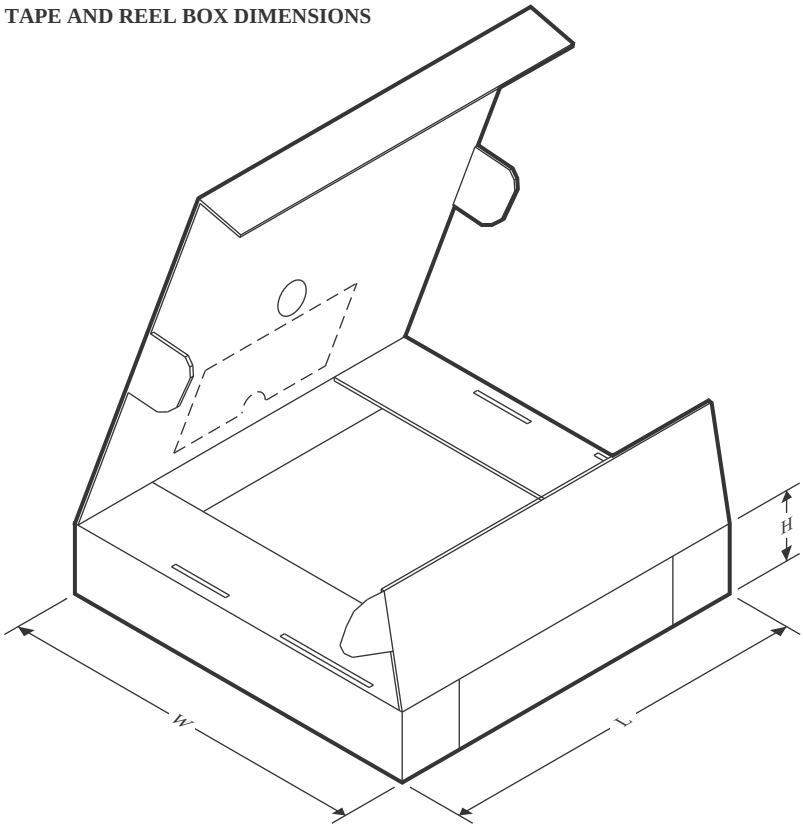
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF411CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

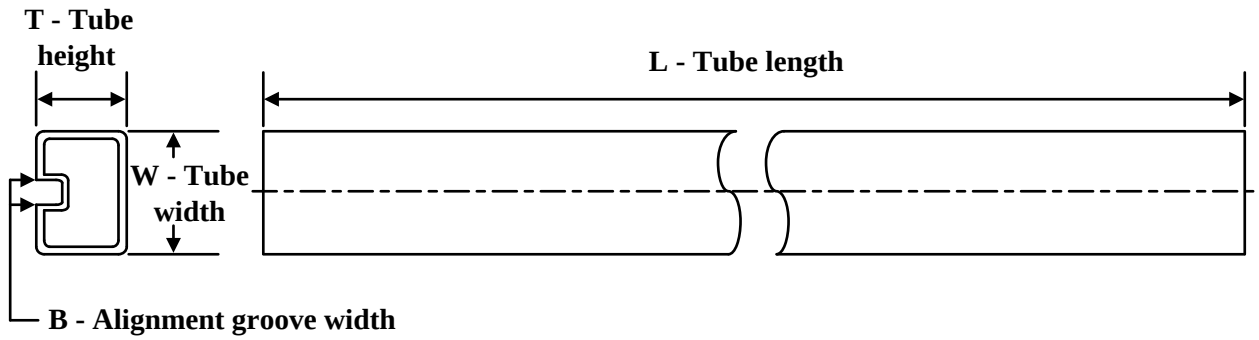
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

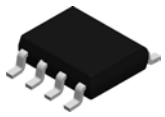
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF411CDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LF411CP	P	PDIP	8	50	506	13.97	11230	4.32
LF411CP.A	P	PDIP	8	50	506	13.97	11230	4.32

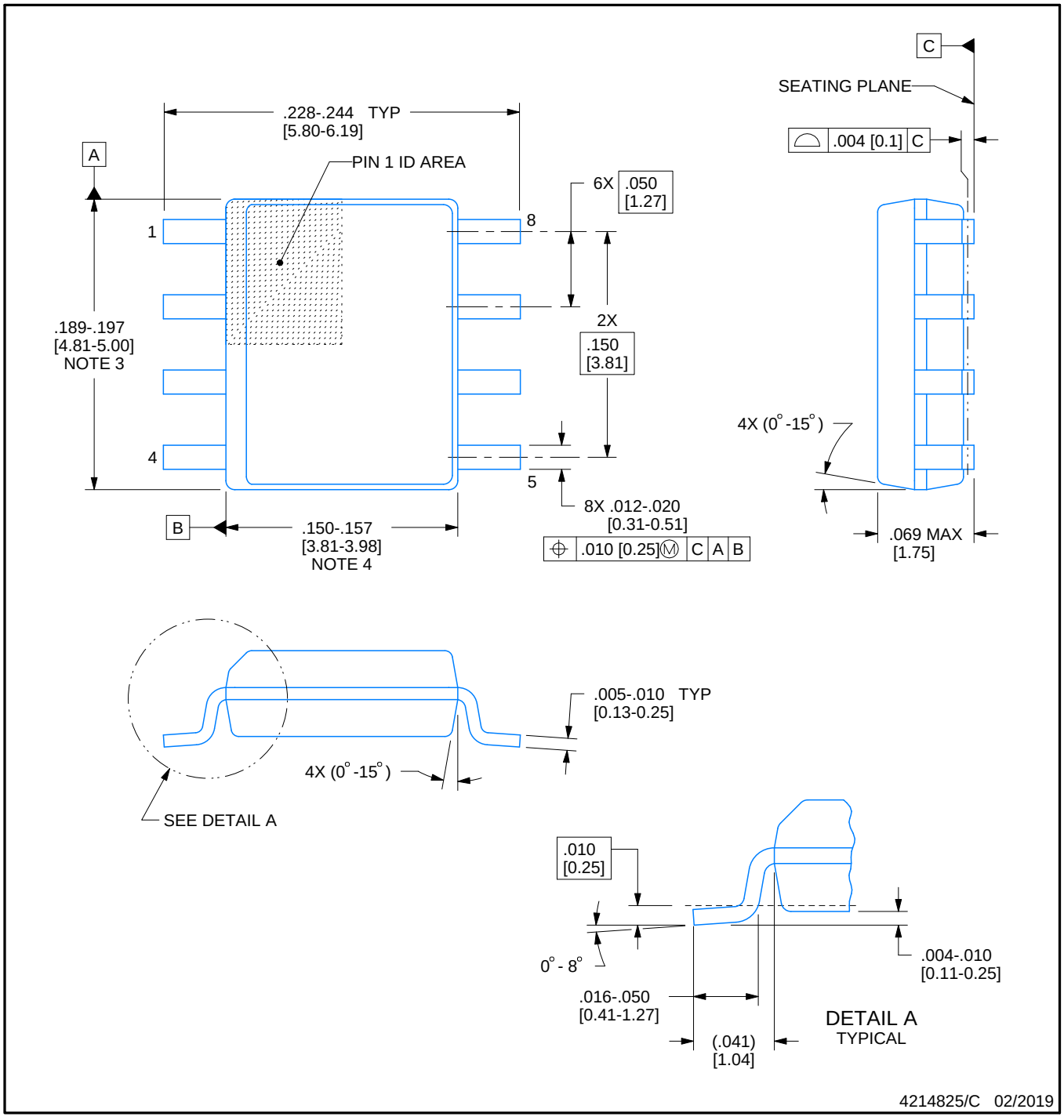


PACKAGE OUTLINE

D0008A

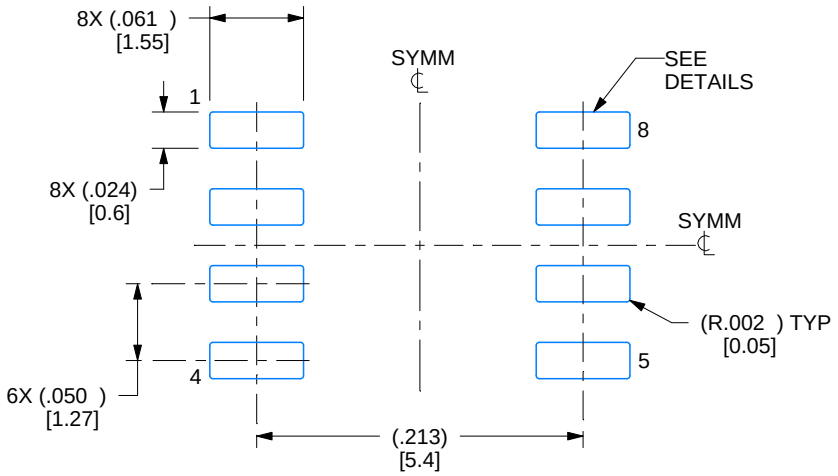
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

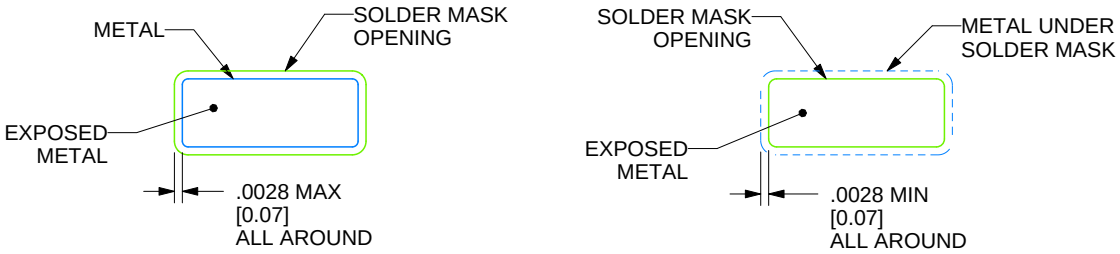


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

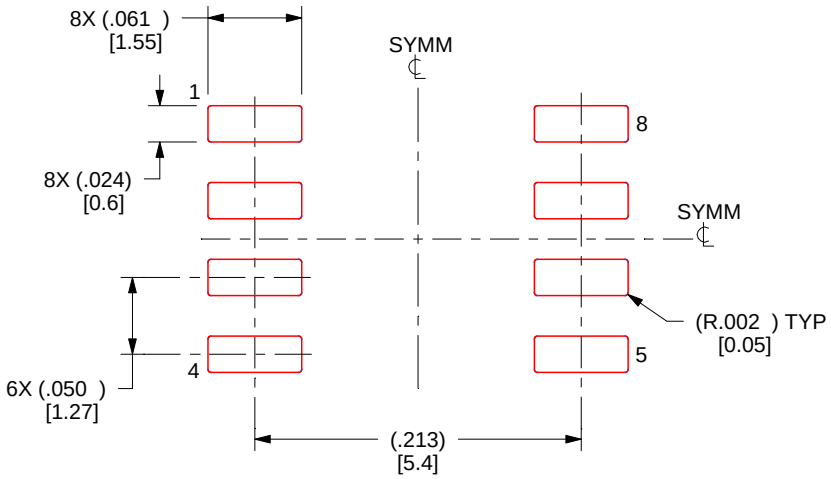
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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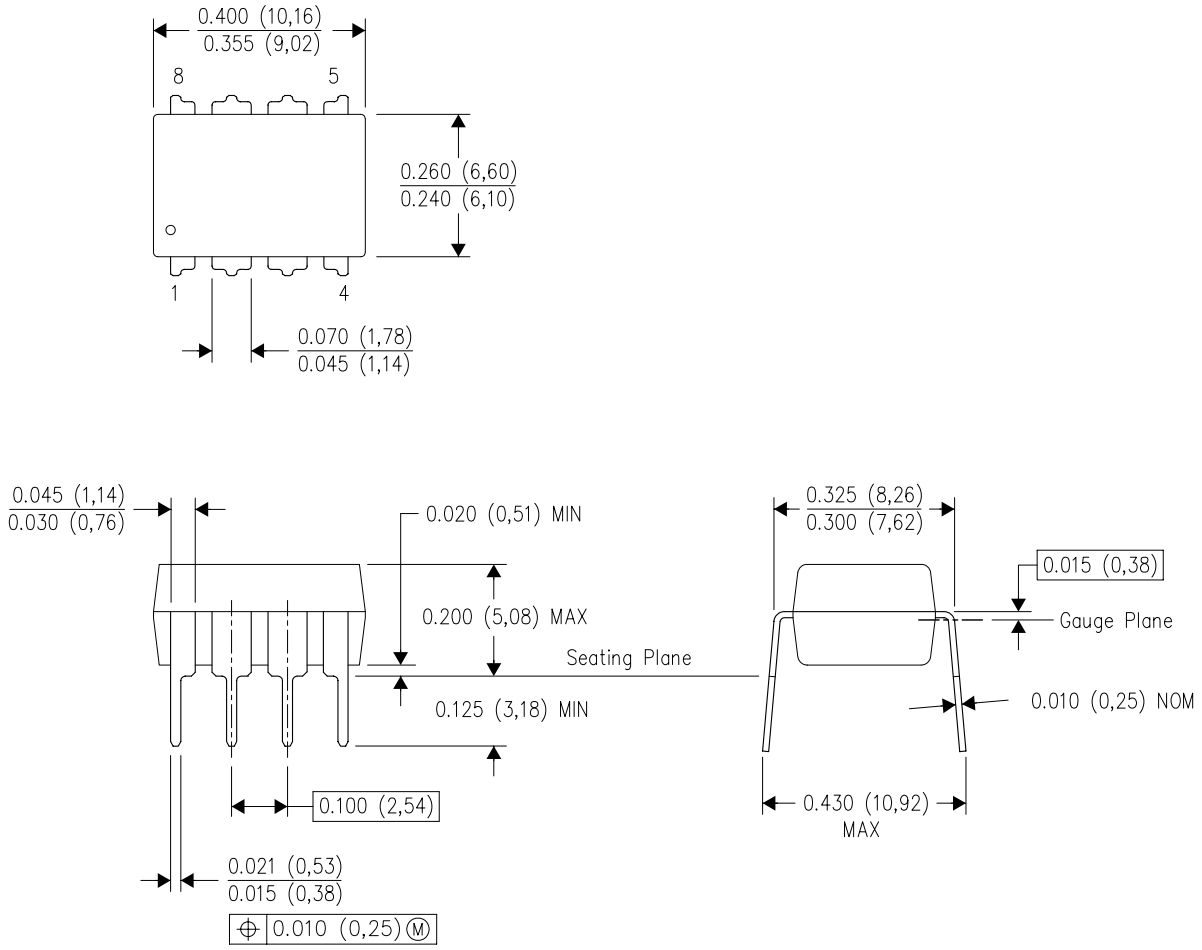
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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